# Advanced Process Control in Semiconductor Manufacturing

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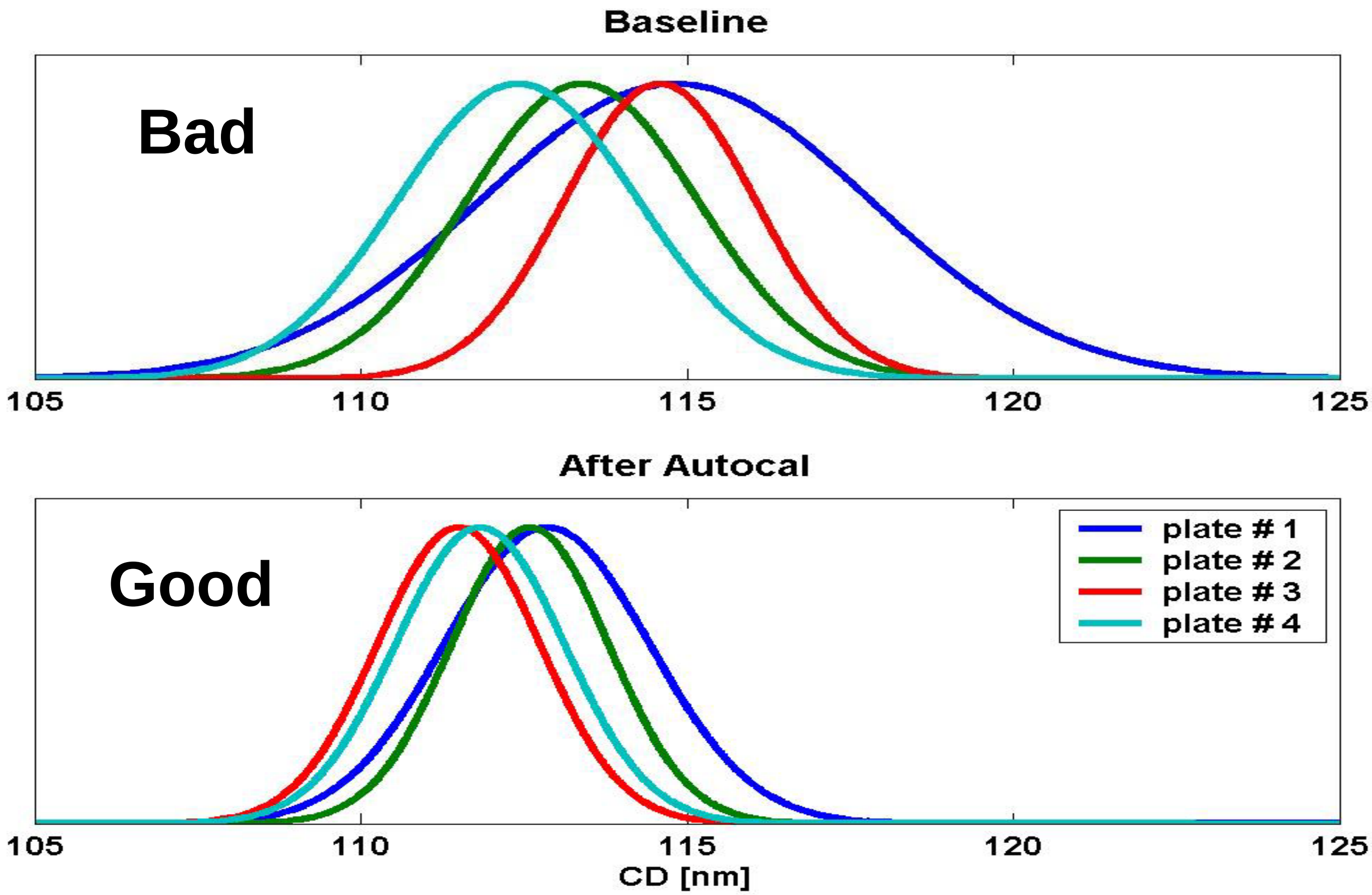
# Outline

- ► The Challenge
- Historical Perspective
- Measuring Variability
  - The Importance of Metrology
- Controlling Variability
  - Applied Concepts – APC at AMD
- Modeling Variability
  - Interaction of Design and Manufacturing
  - Design for Controllability
- Future Perspectives

# Introduction

- Error budgets cannot keep up with shrinking dimensions.
- In the sub-100nm generations, Critical Dimensions (CDs) are hard to control.
  - 65nm features, have an error budget of +/- ~5nm.
  - Often metrology offers about +/- 2nm precision!
  - Processing and metrology equipment are not being built to facilitate integration and control

# The objective is to maintain both Wafer to Wafer and Across Wafer CD Uniformity



# Key Manufacturing Objectives

## *Maximize Revenue Potential of Every Wafer*

**1** **Rock Solid Consistency and Discipline**

***"Zero Uncertainty" in the minds of our customers through consistent on-time delivery of the highest quality product.***

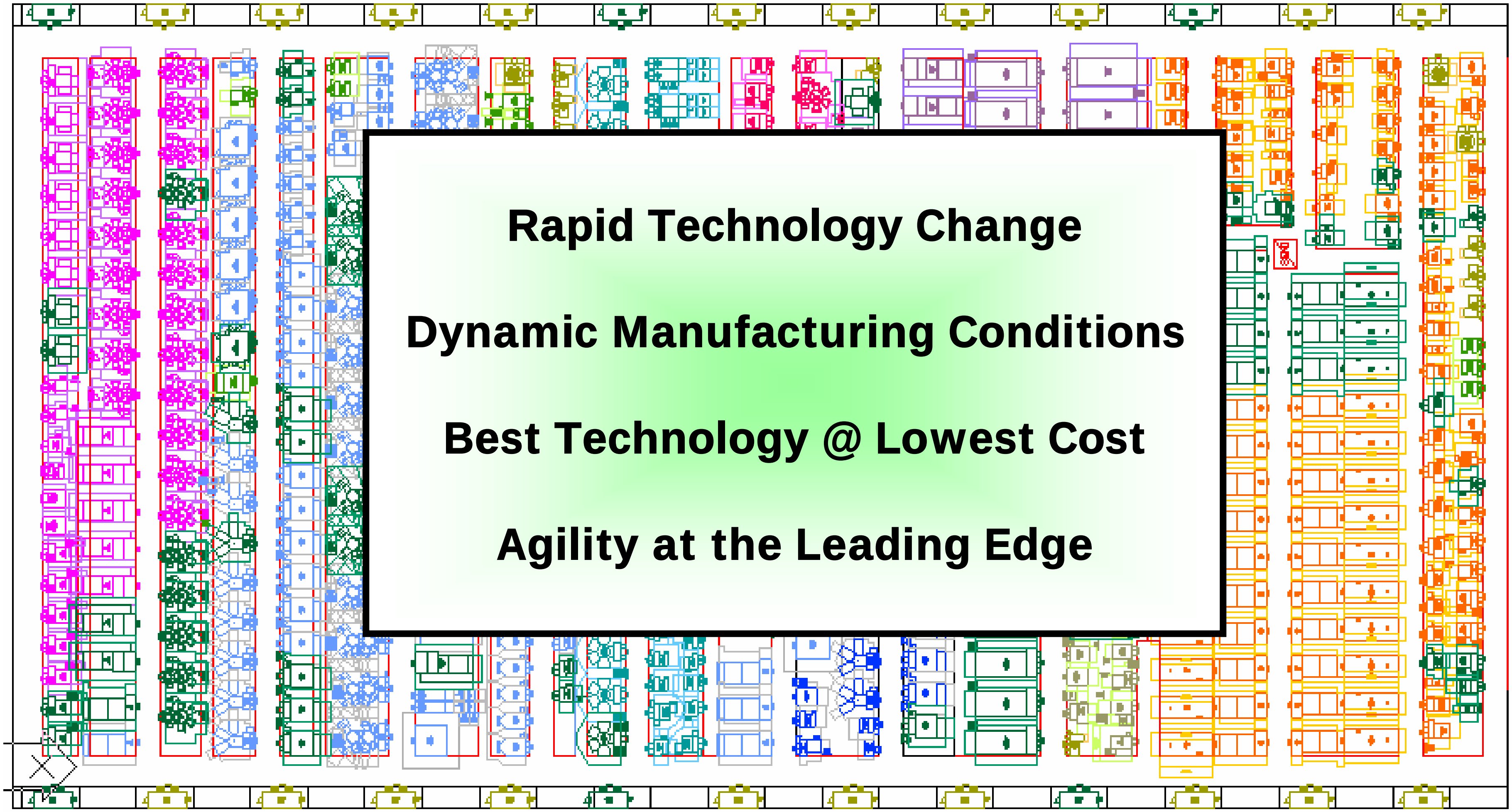
**2** **Maximum Product Performance Through Aggressive Technology Migration**

***Rapid and efficient 90nm transition. Routine transistor improvements to increase product performance without slowing fab output.***

**3** **Minimum Cost Through Industry-Leading Efficiency and Automation**

***Automatic detection and correction of errors in fabs to lower per-die costs. Integrated fab-wide tool communication and control to accelerate time to mature yields on new generations.***

# Constant Push for Performance ...



**Rapid Technology Change**

**Dynamic Manufacturing Conditions**

**Best Technology @ Lowest Cost**

**Agility at the Leading Edge**

# ...in a Non-Stop, High Volume Environment

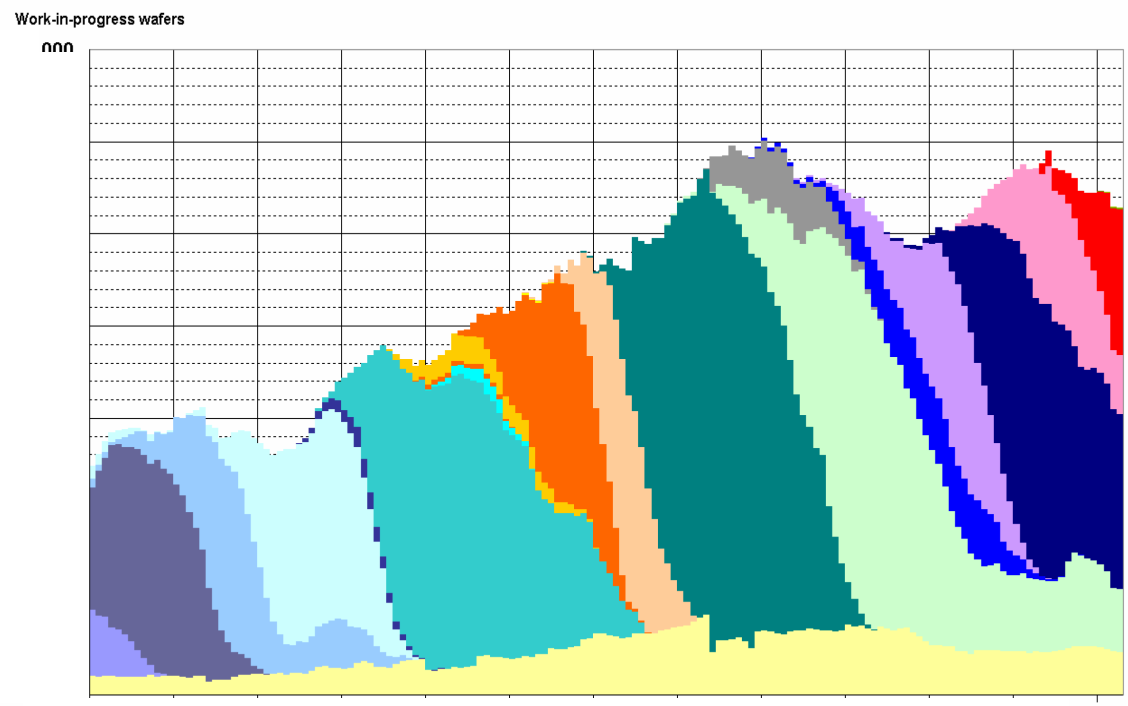
**Mixed mode manufacturing**

**In-fab technology development**

**Enhanced, accelerated cycles of learning**

**Incremental continuous performance improvement**

**Fab 30 WIP by Transistor Node**



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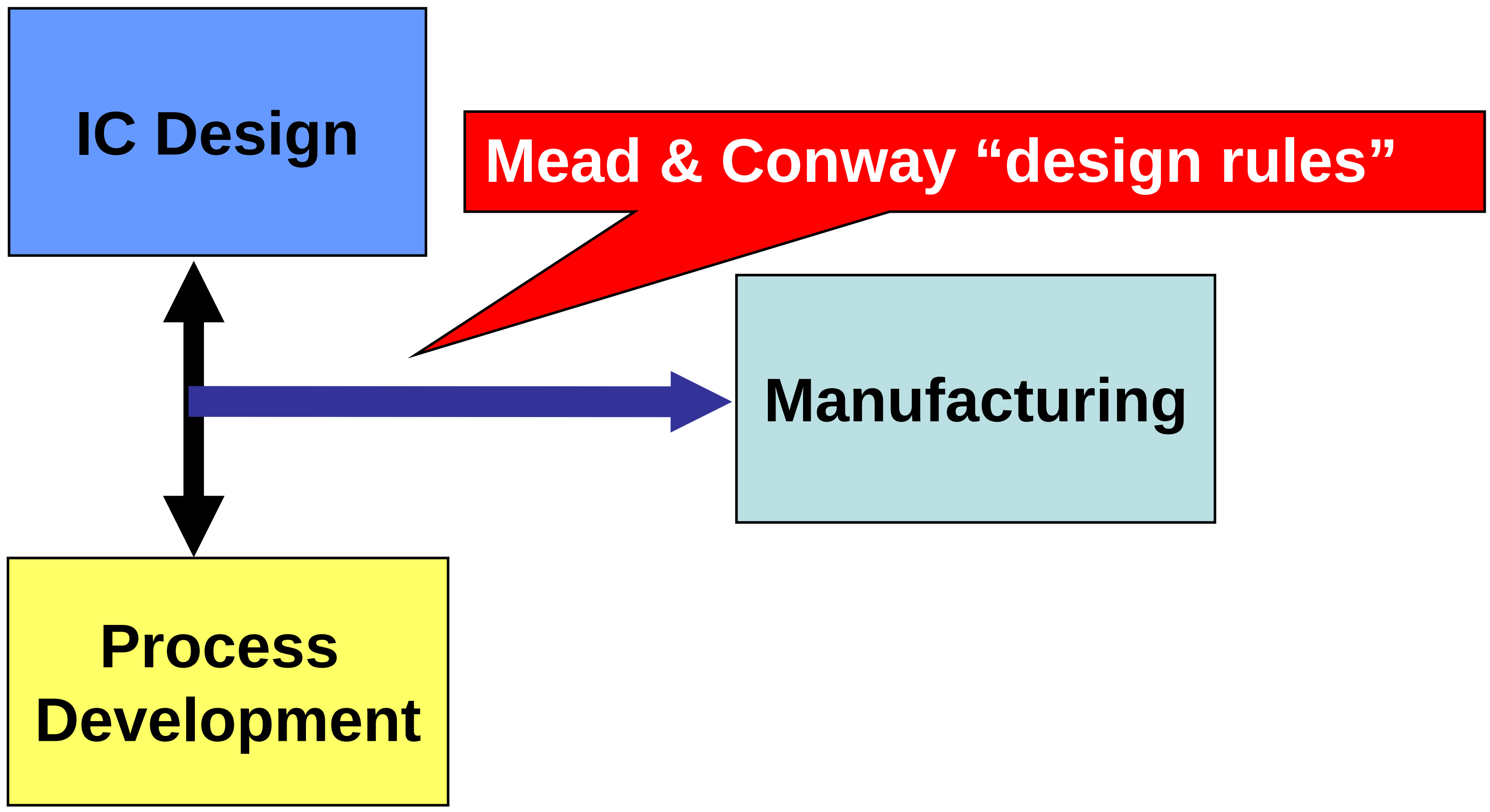
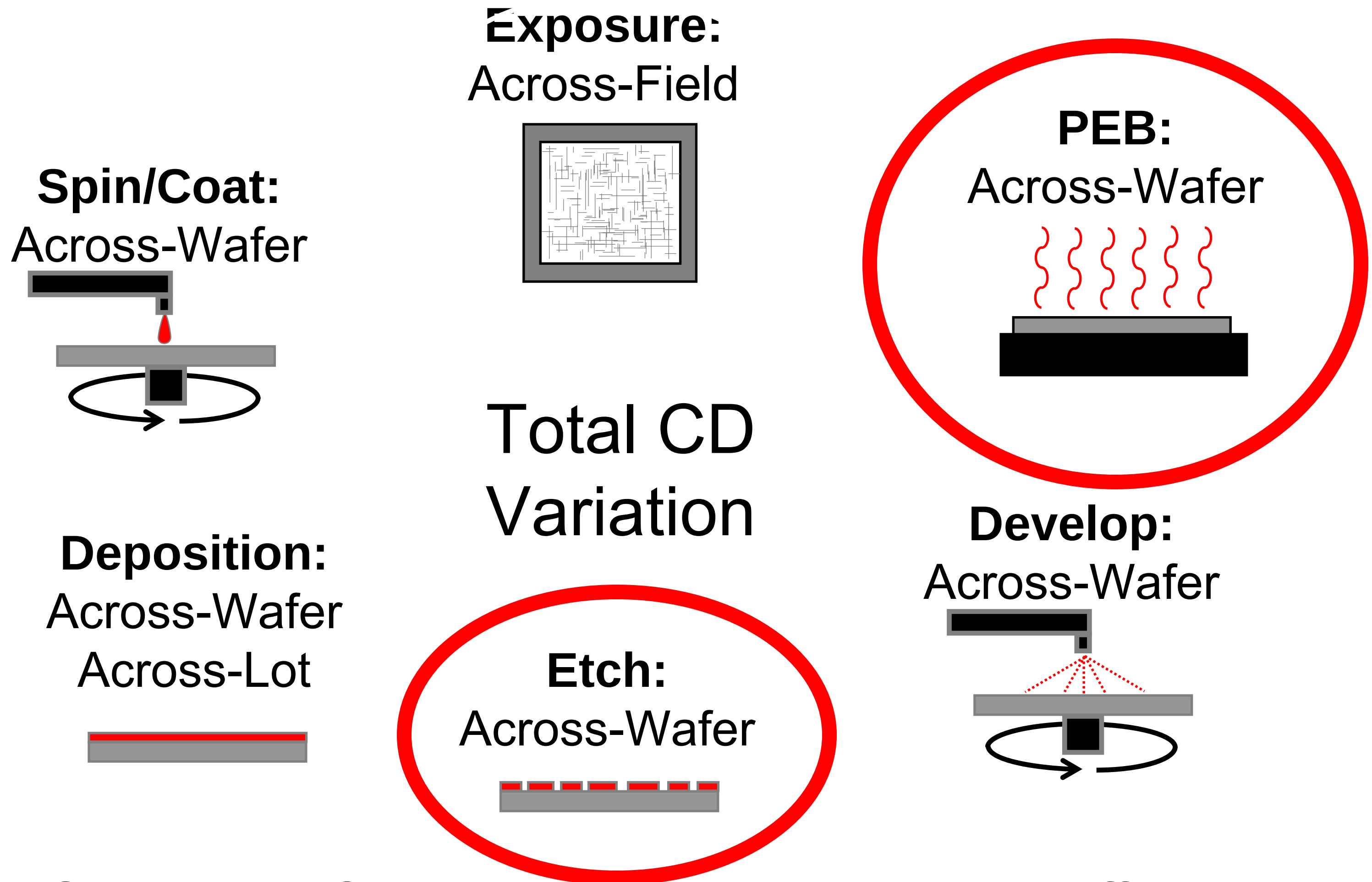
# The Traditional Semiconductor Manufacturing Environment

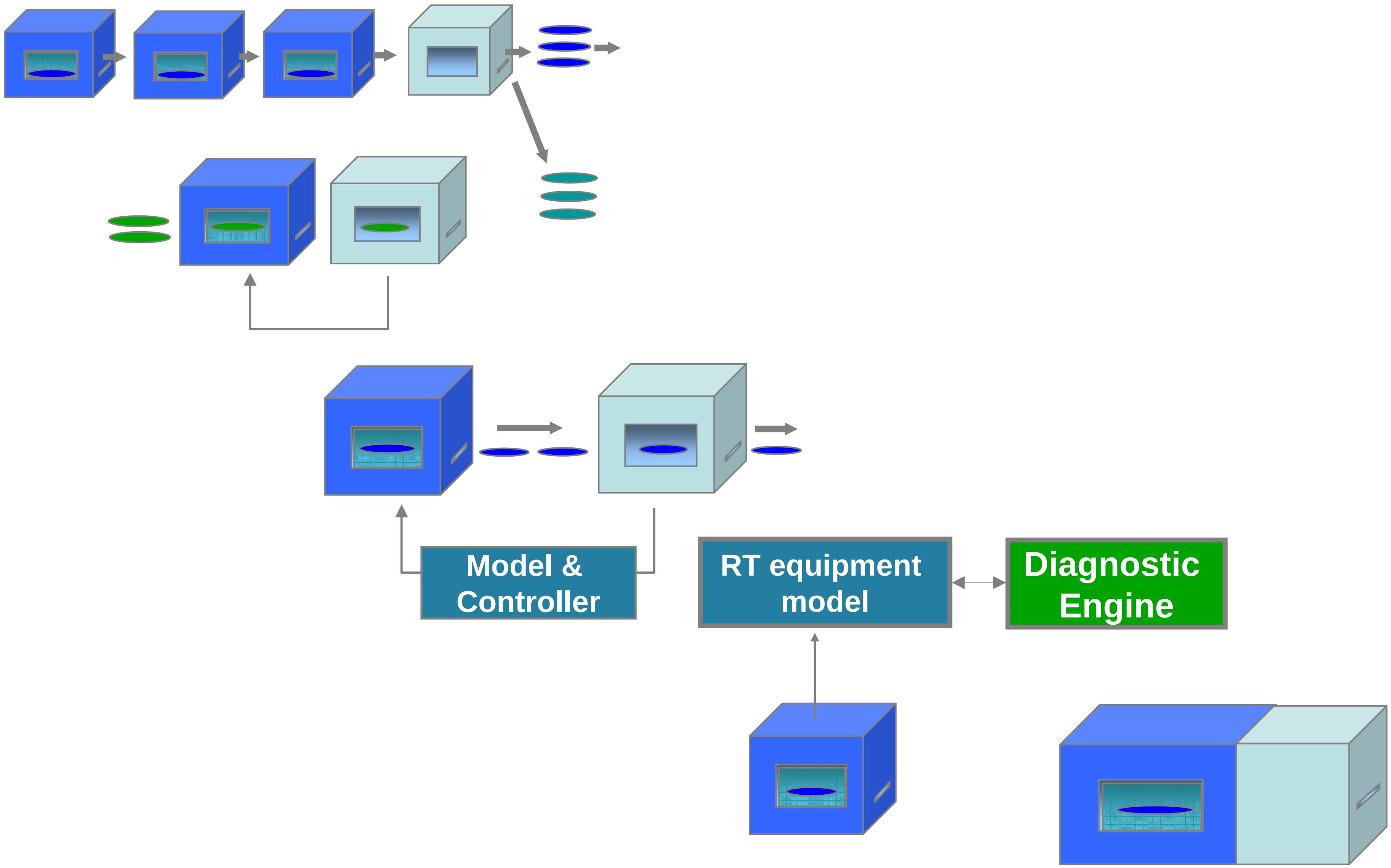


# Sources of CD Variation




Systematic CD variation components with different frequencies are combined.

# Manufacturing Evolution…



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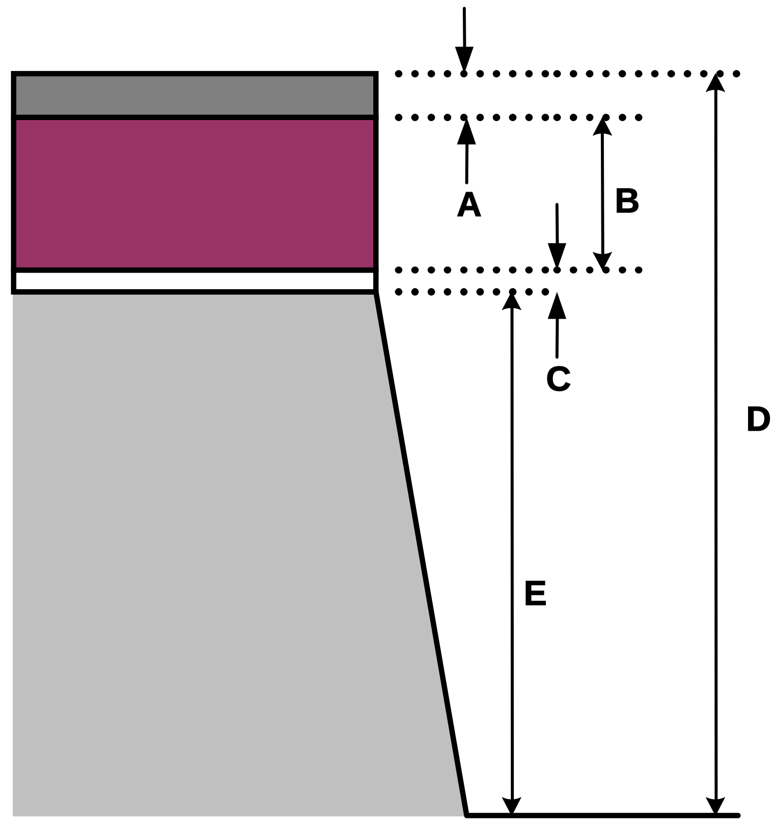
# Metrology Outline

- Metrology tools have been created for inspection and quality control – not for APC.
- CD-SEMs, Optical Metrology, in-situ metrology are advancing rapidly towards an APC/FDC model.
  - Direct metrology error budget remains large
  - The expanding use of indirect metrology requires the introduction of advanced modeling tools in the production line.

# Shallow Trench Isolation Etch Control
## *An AMT-APC Success Story*

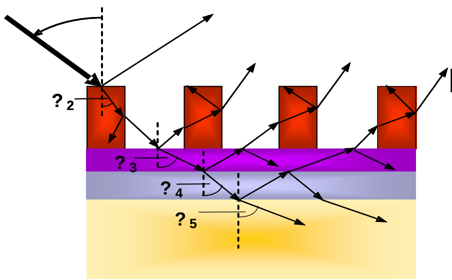
- One of the key metrics for STI Etch control is the depth of the resulting trench into the silicon, but common metrology techniques are unable to directly measure this value.
- Instead, a number of different metrology operations were combined to get an indirect measurement of silicon trench depth.
- The noise from each of these measurements was added to the signal being used for automated control.
- AMT and APC decided to explore scatterometry as an alternative metrology

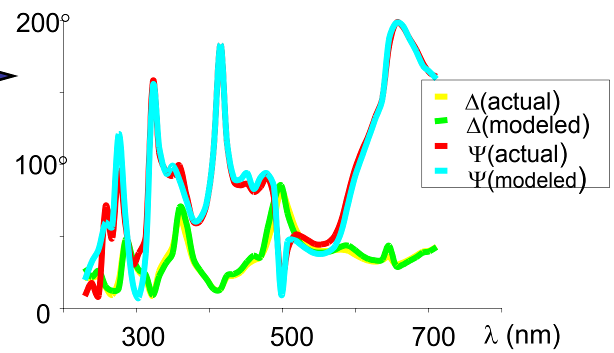


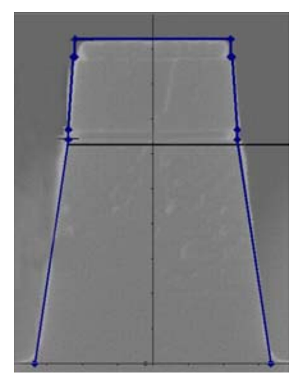

**A = ARC Thickness (Optical)**
**B = Nitride Thickness (Optical)**
**C = Barrier Oxide (Optical)**
**D = Trench Depth (Profilometer)**
**E = Derived Silicon Depth**

# Advanced Measurement Technology
## *Scatterometry for STI Etch Production*

- Efforts continue to evaluate and implement advanced measurement technology for production solutions
  - New metrology (e.g. scatterometry)
  - Sensor solutions
  - Etc…
- The implementation of scatterometry for STI etch control in FASL Fab 25 was one of the first large-scale uses of scatterometry in a production semiconductor manufacturing facility.



# Shallow Trench Isolation Etch Control

## *An AMT-APC Success Story*

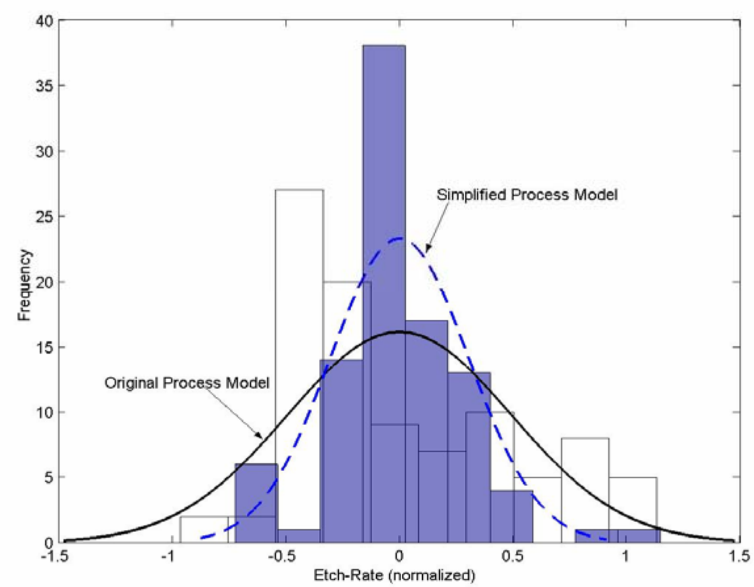
- Reduced Uncertainty
  - Precision

    *Scatterometry represents a 5x improvement in precision compared to the profiler*
  - *Accuracy*

    *Scatterometry measures at design rule spacing instead of a large isolated test pad*
  - *Stability*

    *Scatterometry hardware does not drift like the contact profiler*
- Created New Capabilities
  - Direct measurement of silicon depth (no feed-forward derivation)
  - Combined CD, profile, and thickness metrology

- Results
  - Improved Control
    - Cpk improvement of 90%
  - Reduced Cost
    - Eliminated feed-forward metrology
  - Improved Cycle Time
    - 3x faster metrology system



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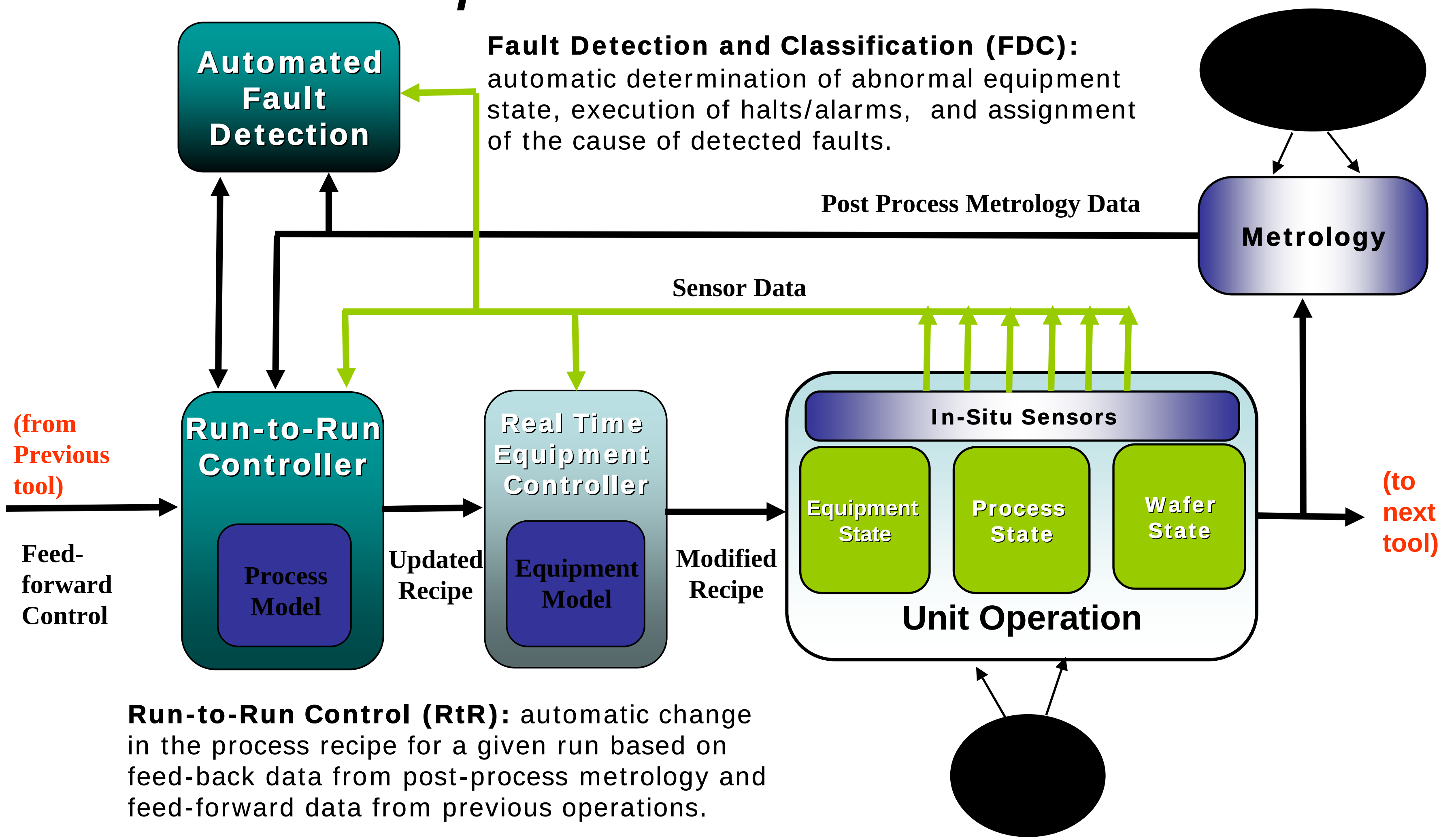
# Advanced Process Control

## *APC incorporates RtRPC and FDC*

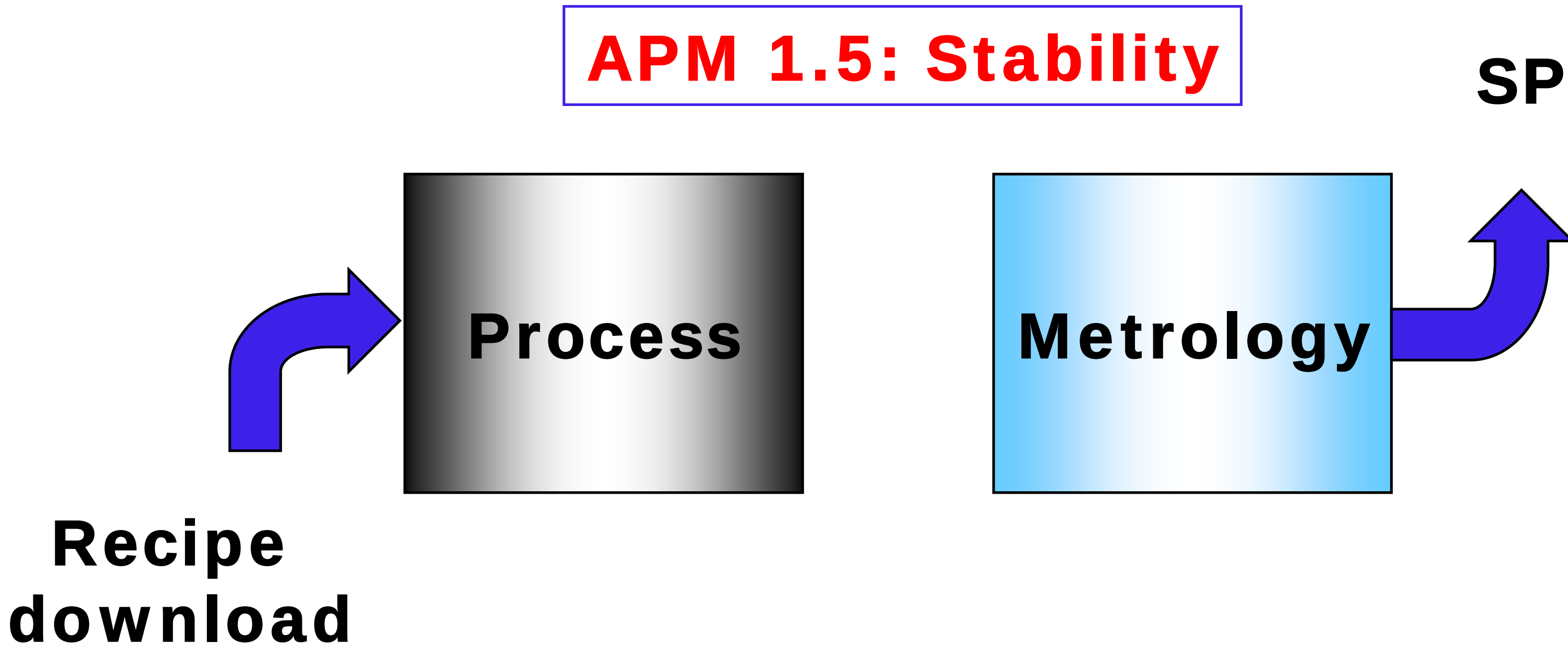



**Fault Detection and Classification (FDC):** automatic determination of abnormal equipment state, execution of halts/alarms, and assignment of the cause of detected faults.

**Run-to-Run Control (RtR):** automatic change in the process recipe for a given run based on feed-back data from post-process metrology and feed-forward data from previous operations.

# Automated Precision Manufacturing

*Control Evolution*

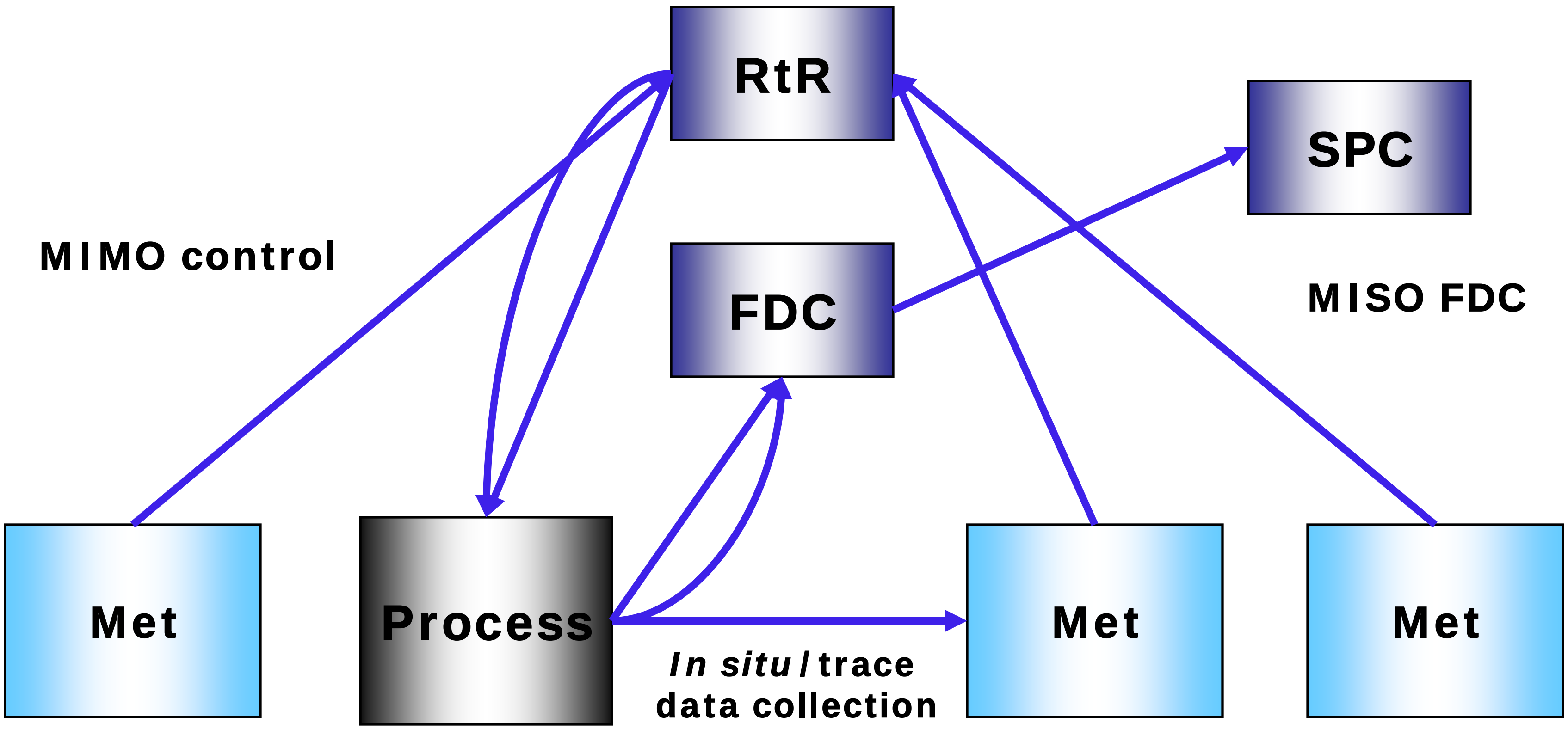



- Automated recipe download through an Equipment Interface minimized process setup errors and improved productivity.
- Statistical Process Control provided visibility into and control of run-to-run stability of each process.

# Automated Precision Manufacturing

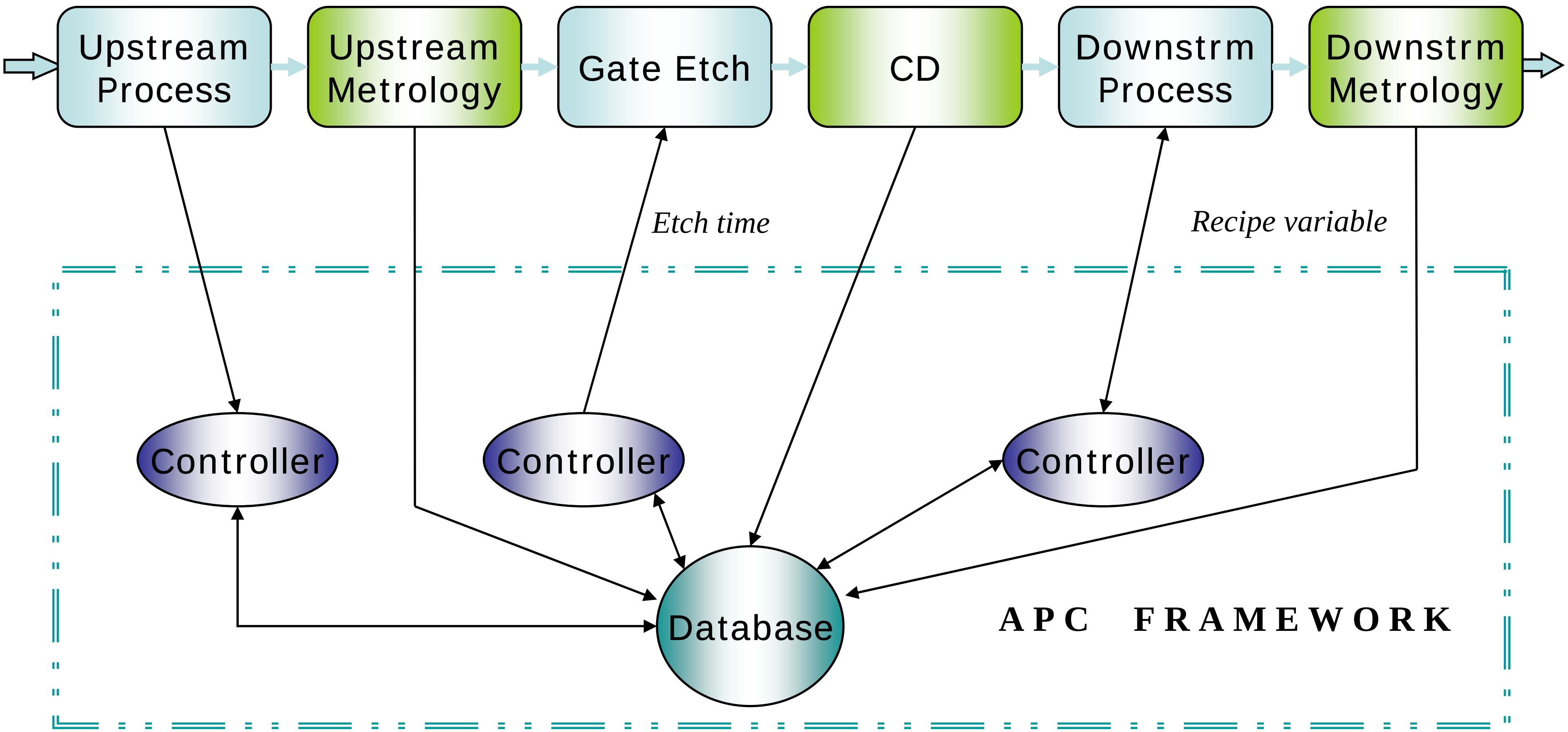
## *Control Evolution*

**APM 2.0: Controllability**



# Transistor Control

## *Gate Etch Control with FF/FB Control*



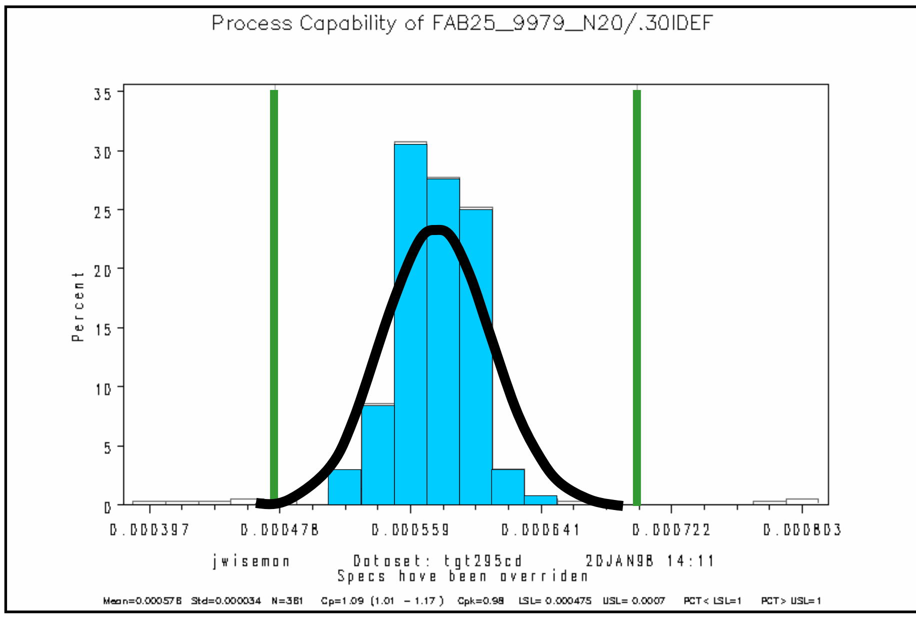

- Resist trim etch control, along with controls at upstream and downstream operations, effectively control drive current according to our understanding of device physics.

# Transistor Control

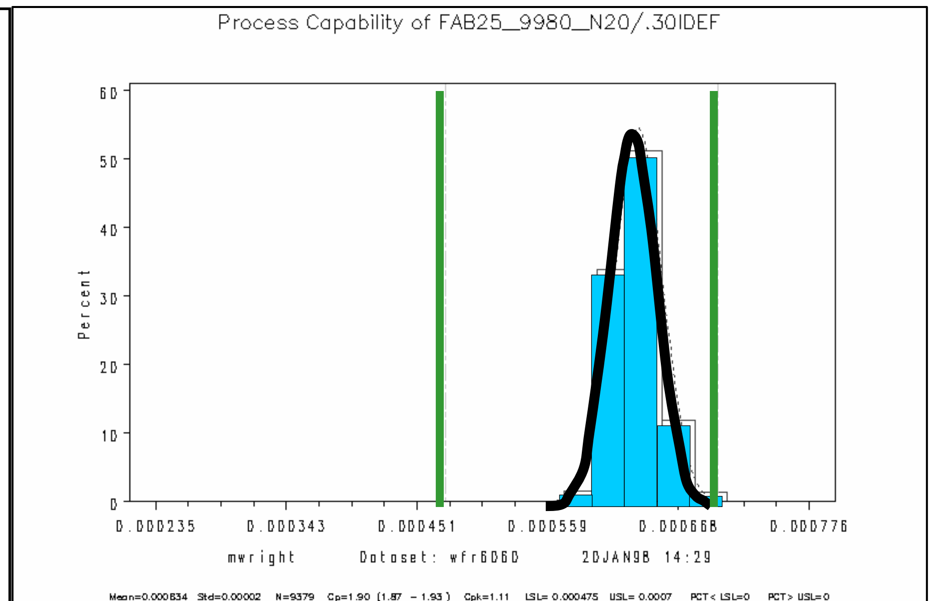
## *Effect on Microprocessor Speed Distributions*

Initial Impact of APC on MPU Performance – 1998 – Narrower transistor drive current distribution allows AMD to push our process to the edge of the spec without fallout for high power or slow parts

AMD-K6® drive current distribution before Id,sat control




AMD-K6® drive current distribution after Id,sat control

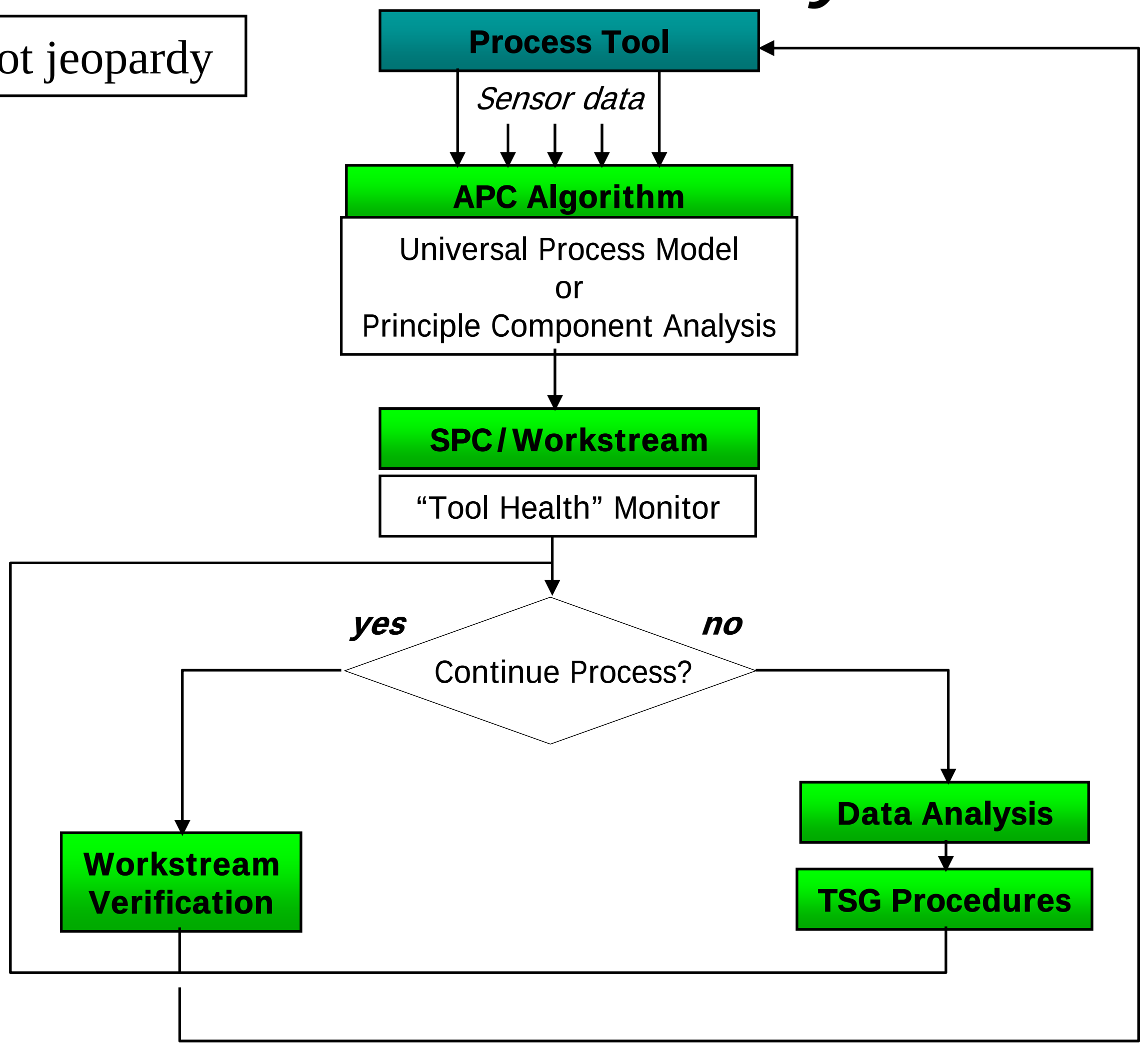



**Initial side-by-side comparison: Leff APC used ever since in F25 and from start-up in F30**

# Fault Detection and Classification

## *MISO FDC Analysis*

Goal: single lot jeopardy

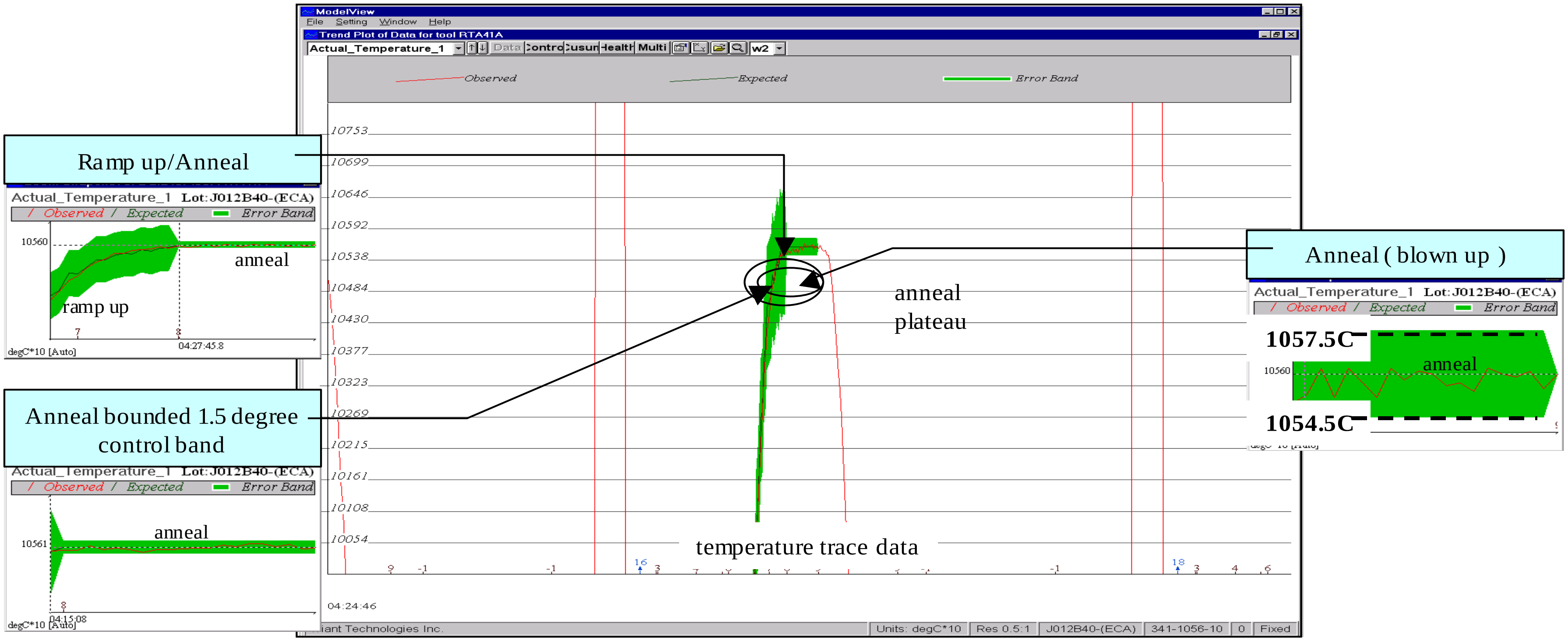


# Fault Detection and Classification

## *Rapid Thermal Anneal FDC*

FDC model tightened control beyond manufacturer's specifications to + 1.5 °C alarm limits (3-σ)

"Temp_probe_1" trace is bounded by a +/- 1.5 degree control-band (green ) in real-time during last half of the anneal at target temperature.

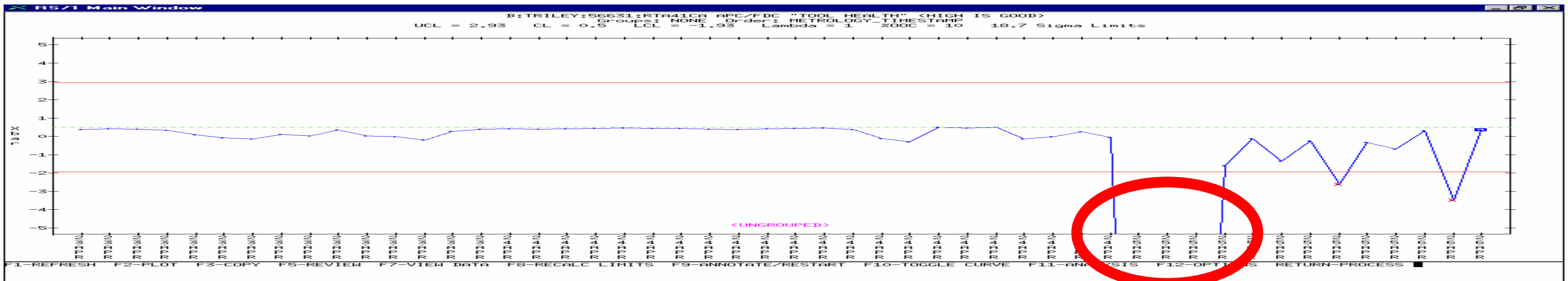


# Fault Detection and Classification

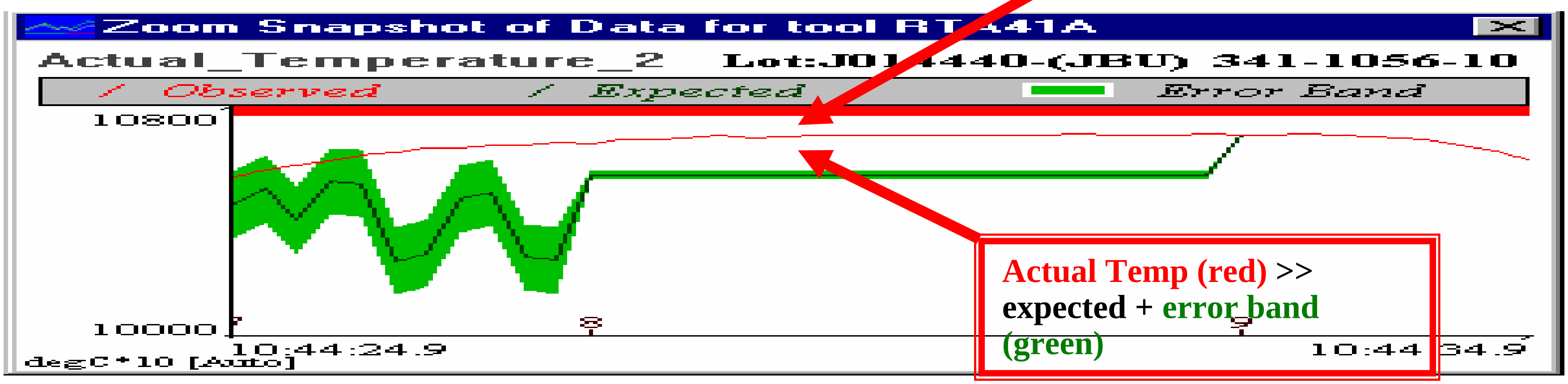
## *RTA process monitoring and interdiction*

AMAT RTA Fault Detection & Classification

Chart Caught RTA41A Zone 2 Temp Problem (14° C Too High)



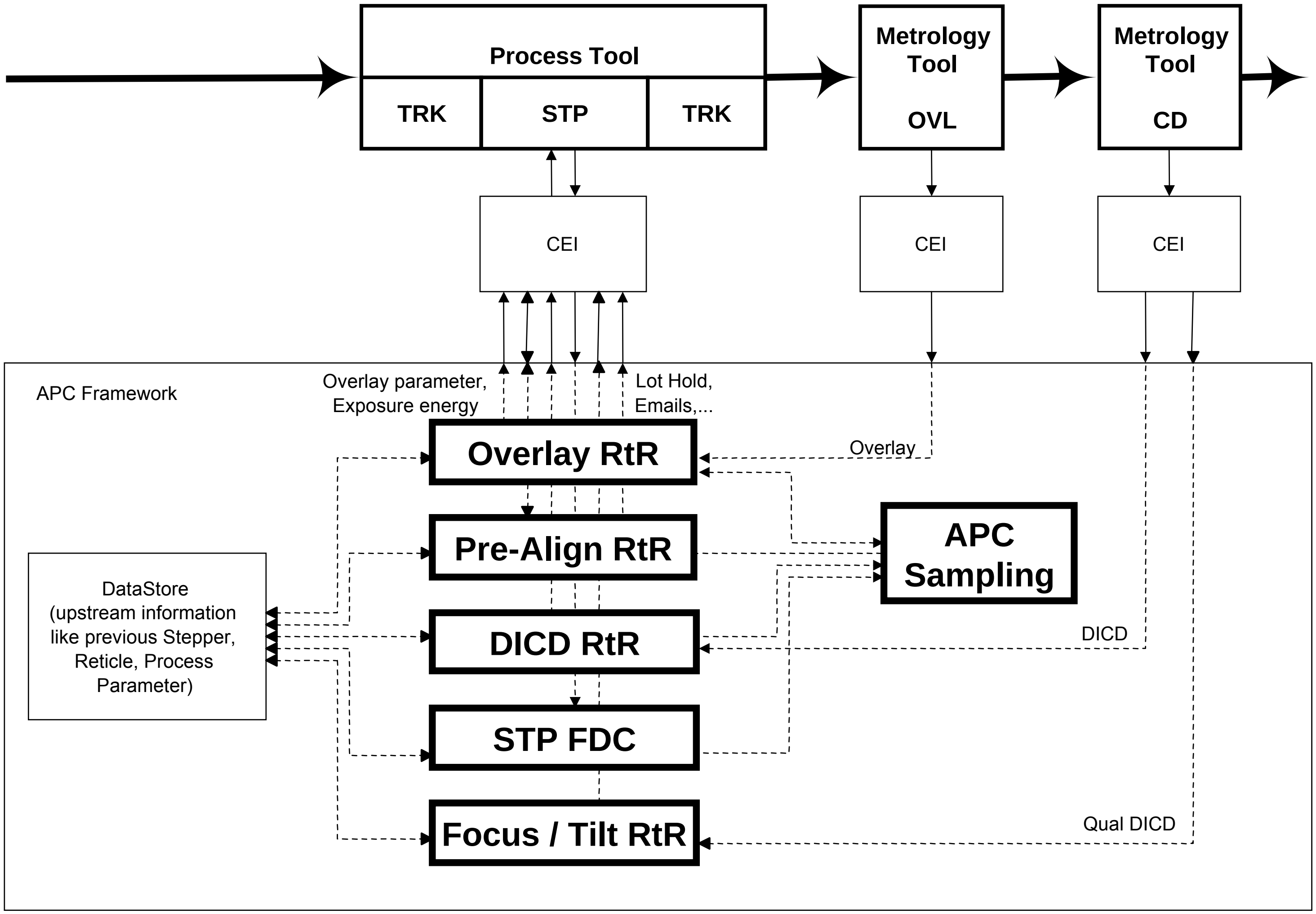
*Workstream chart reconstructed to reflect current, proper, LCL to reduce false fails*




***Bottom Line: Achieved a 86% reduction in product lot risk***

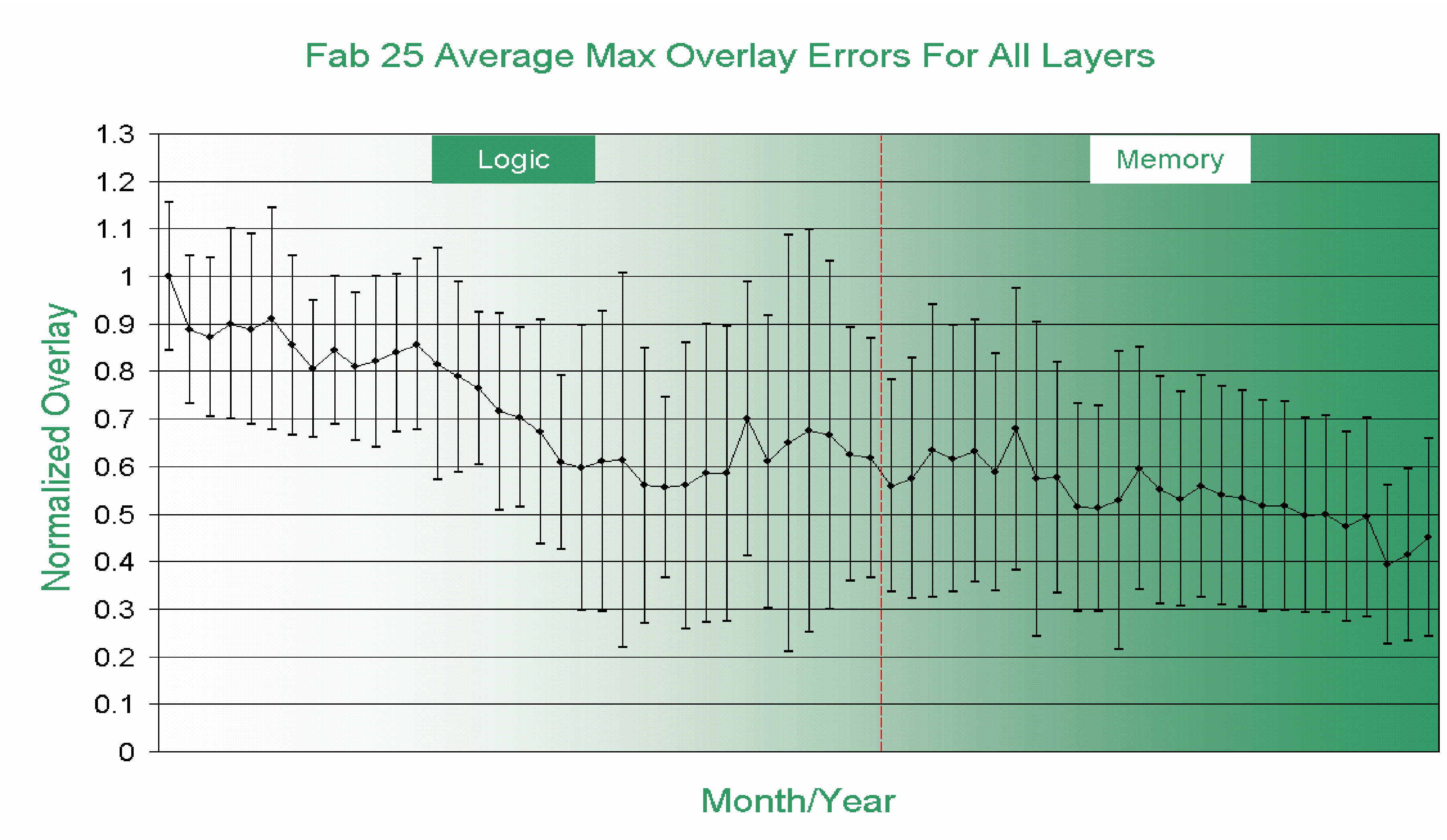
# Lithography Control

## *Schematic of Integrated APC Applications*



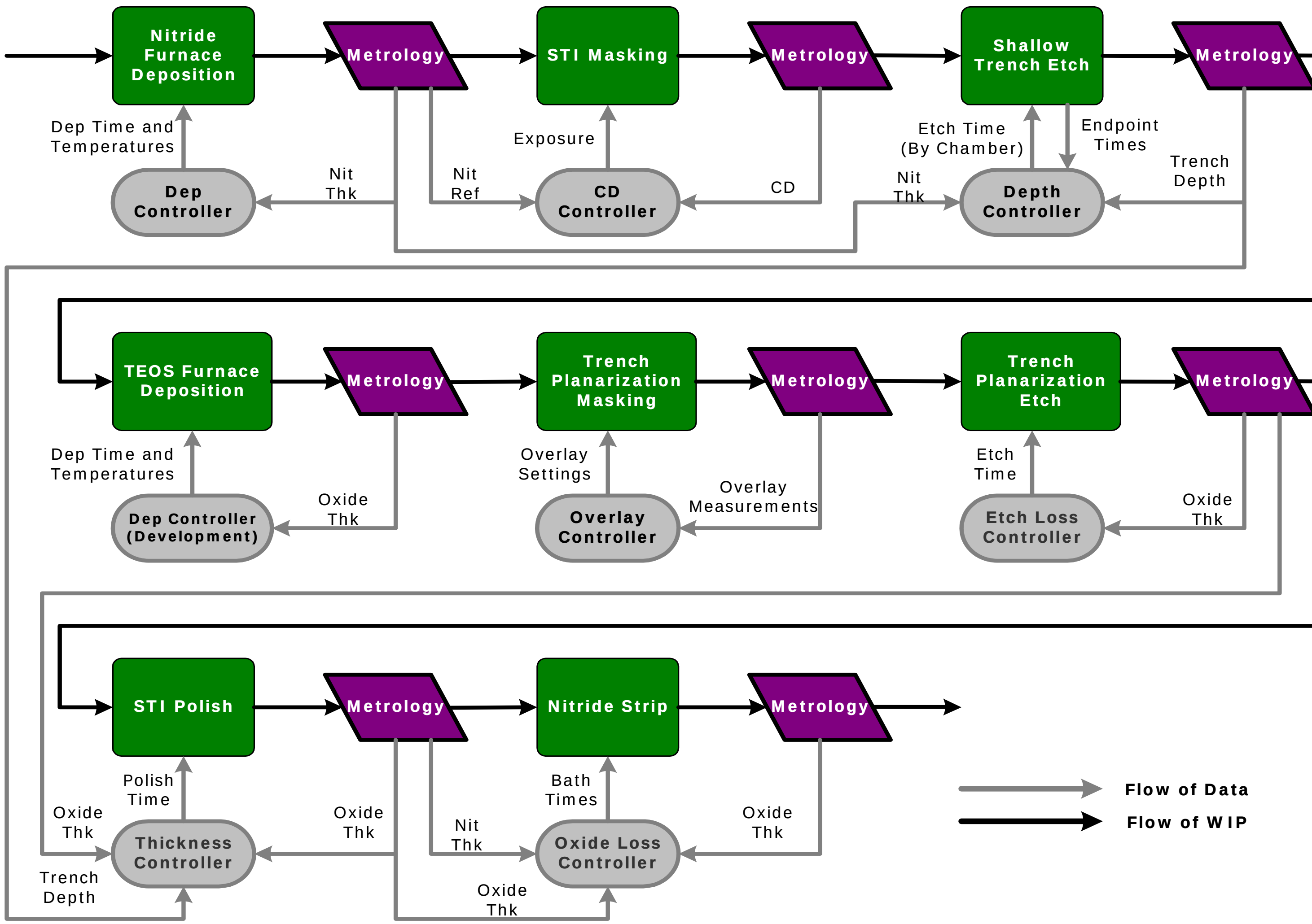
# Lithography Overlay Control

## *Performance improvement over 6+ years*



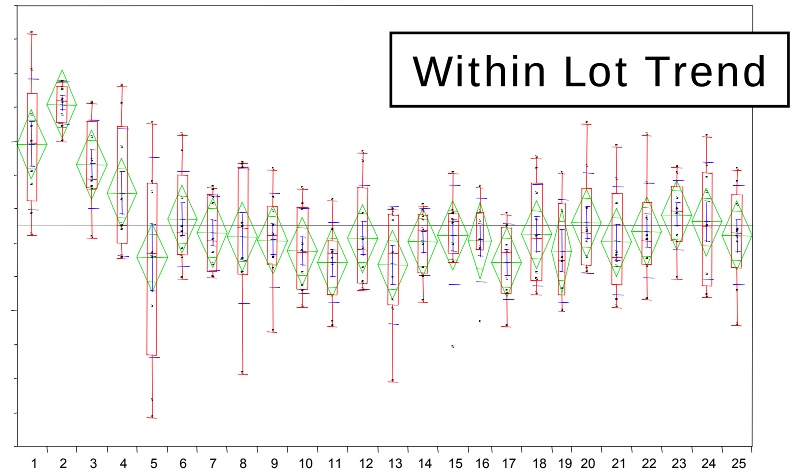
# Islands of Control

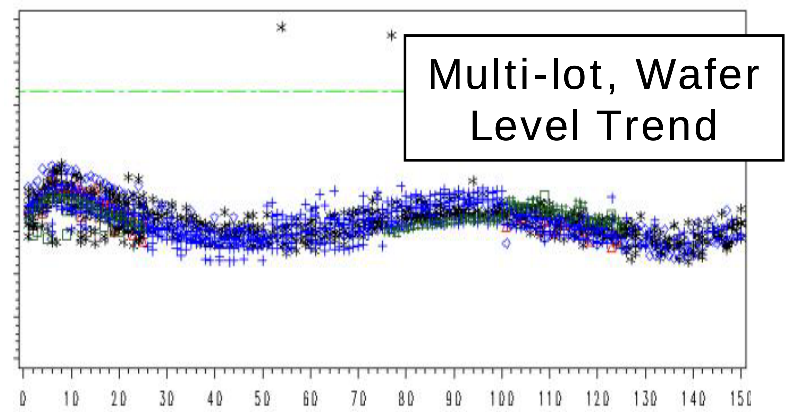
## *FASL Fab 25: Shallow Trench Isolation*



# The Need for Wafer Level Control

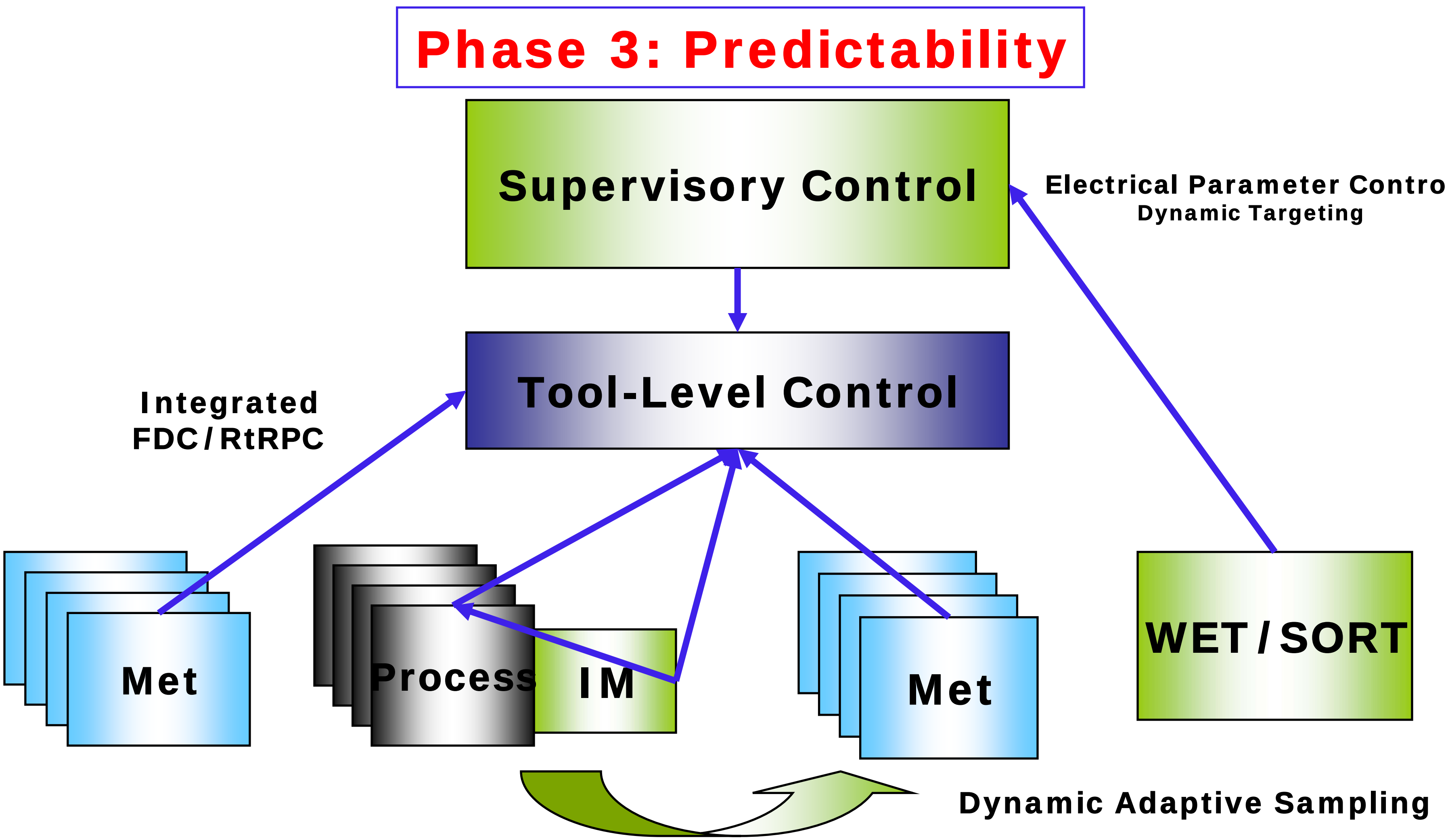
- Processes within the factory exhibit drift that show repeatable signals within the lot or over larger periods.
- With the higher costs of 300mm wafers and processing, the economic impact of this variation is not acceptable.
- Wafer level control applications can be used to eliminate much of this variation and thereby improve the economics of the factory.



# Automated Precision Manufacturing

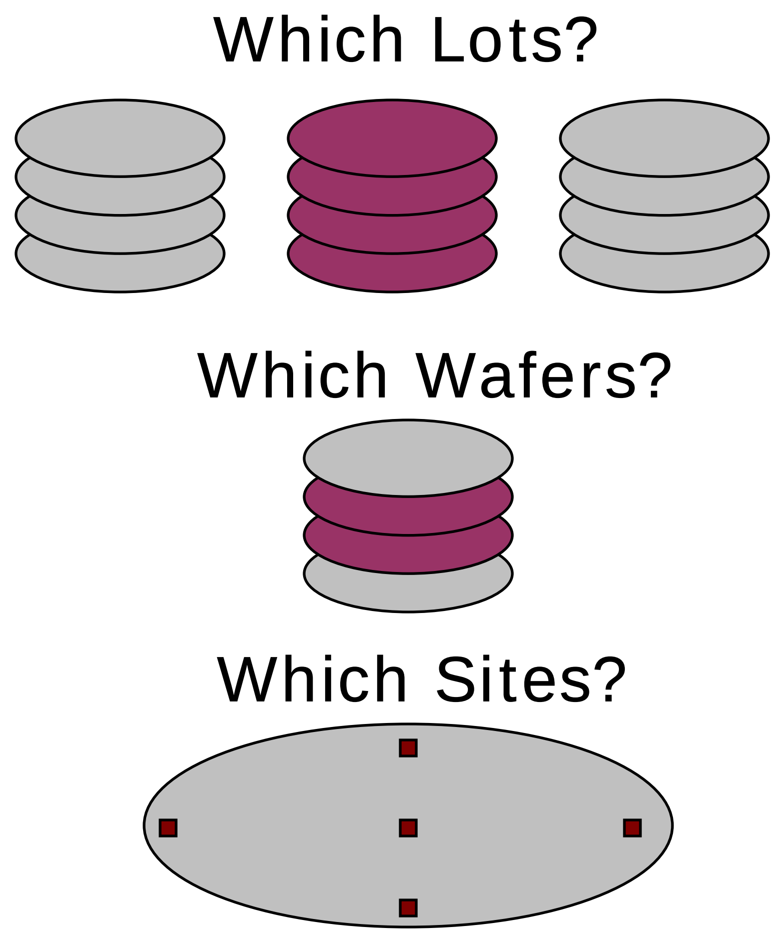
## *Control Evolution*



# Fab-Wide Control Technology

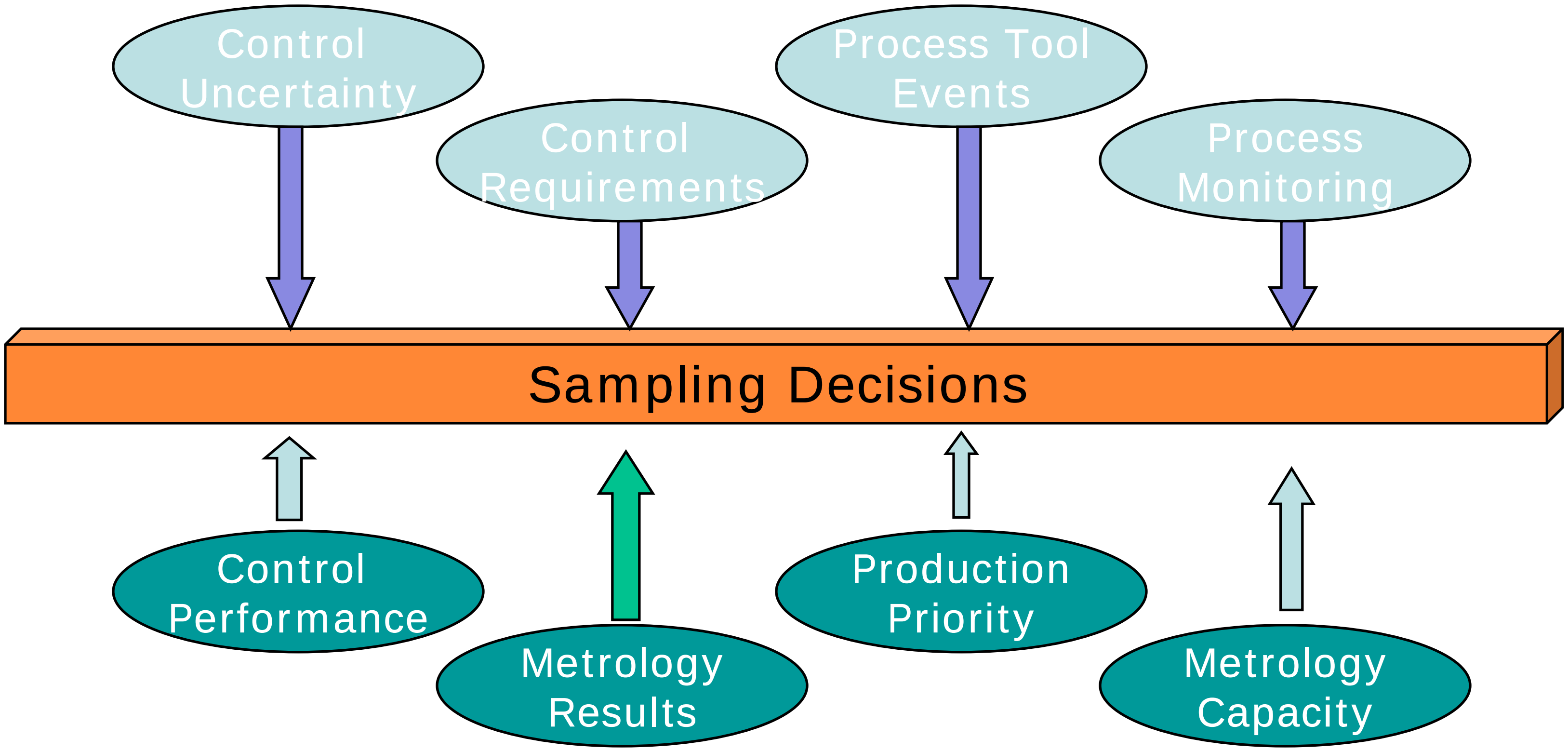
## *Dynamic Adaptive Sampling*

- Like dispatching, the decisions on what type of metrology sampling also could benefit from the inputs of an APC application.
- This input could impact all levels of sampling:
  - Do you measure a particular lot?
  - Do you measure a particular wafer in a lot?
  - What is the pattern of sites on the wafer?
  - What structures should be measured at each site?



# Fab-Wide Control Technology

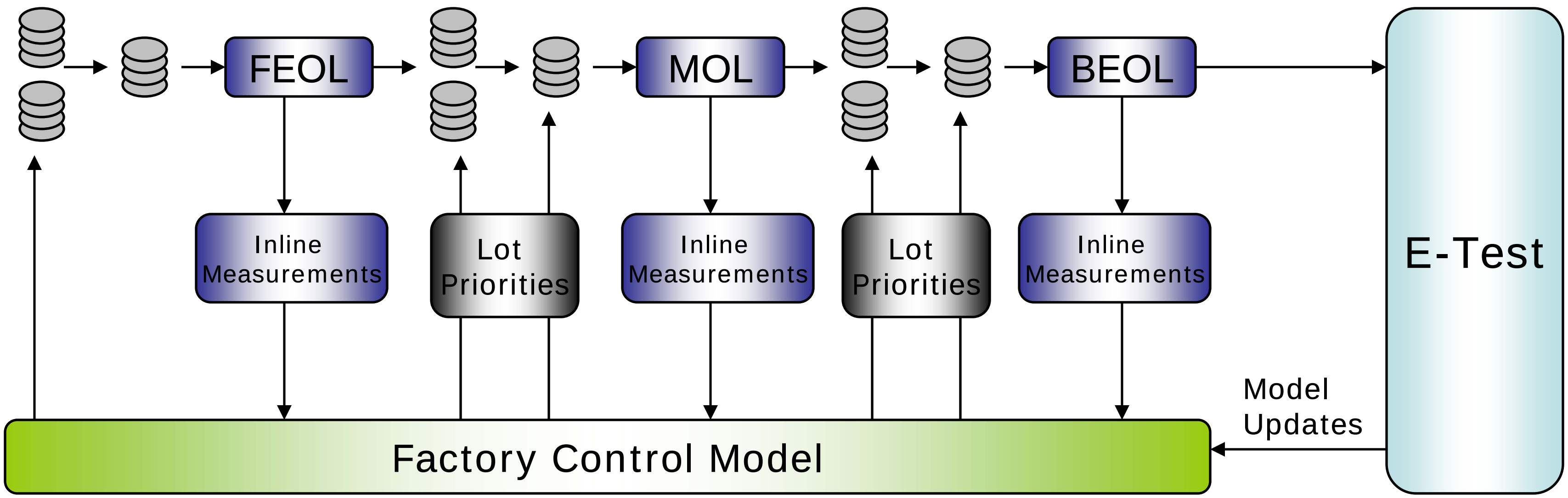
## *Factors Influencing Sampling*




Incorporation of control related inputs allows for “smarter” sampling based on factory performance.

# Fab-Wide Control Technology

## *Dynamic Production Control*




**Determine speed distribution** for each lot based on in-line measurements and transistor model

**Change priority** of lot based on estimate of # of parts in speed bins and production outs requirements (based on user input of outs@speed / week)

**Change equipment set** for each lot based on equipment performance (defectivity, speed impact) and requirements for outs

**Change starts** based on current estimations of in-line yield@speed and requirements for outs

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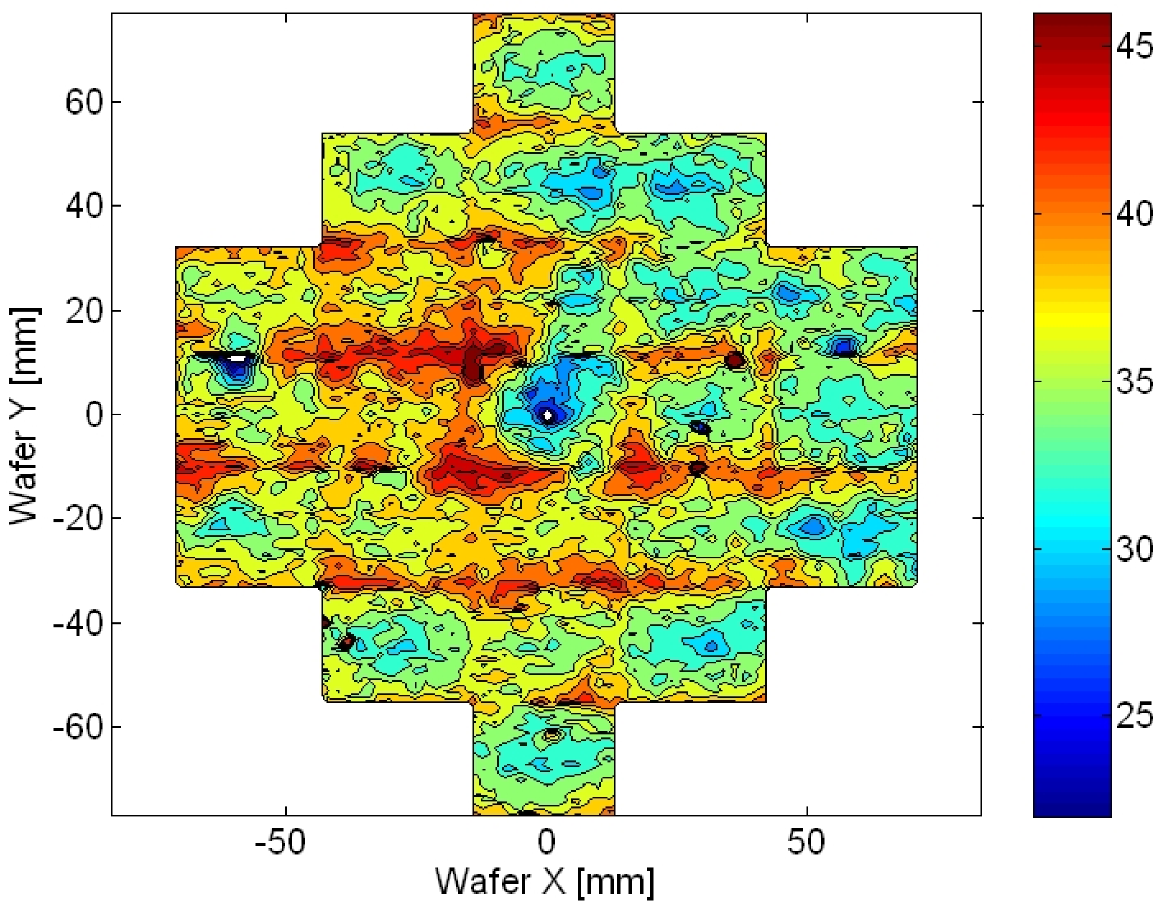
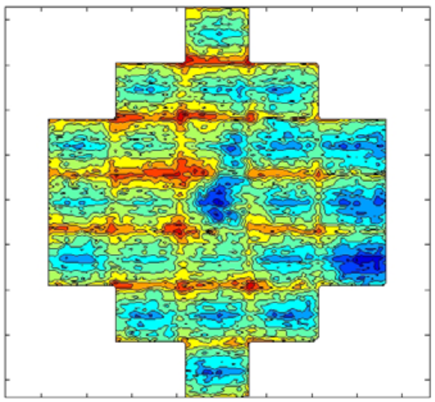
# Spatial Correlation Analysis

Exhaustive poly-CD measurements (280/field):

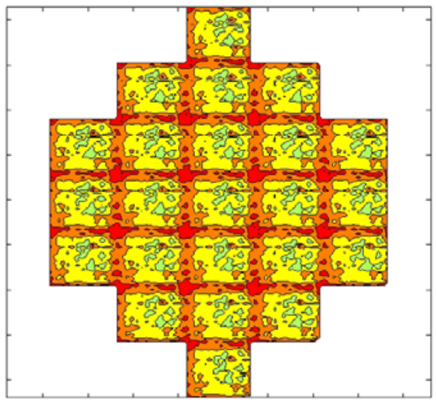


# Origin of Spatial Correlation Dependence



Average Wafer

-



Scaled Mask Errors

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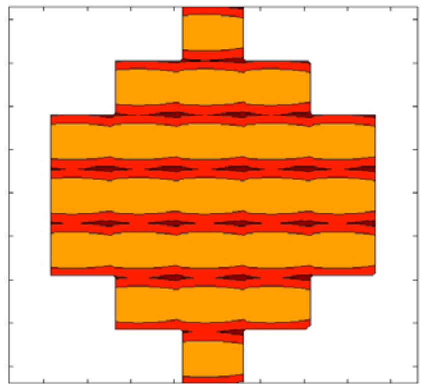

Across-Field Systematic Variation

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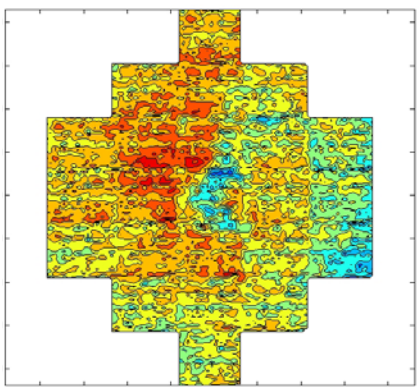
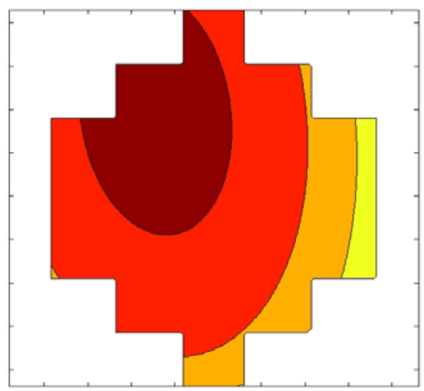


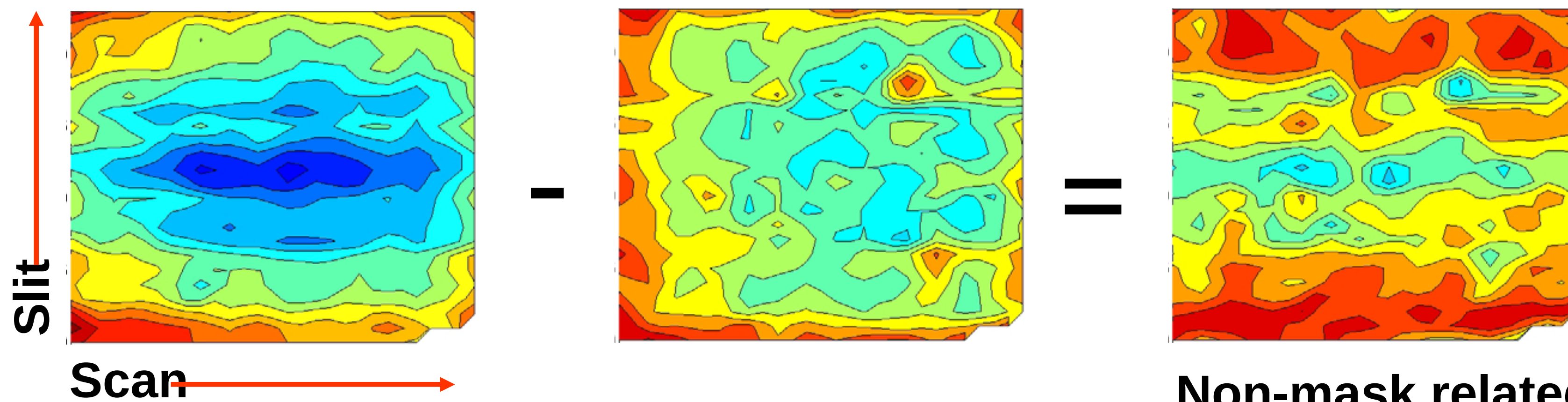
**Across-Wafer Systematic Variation**



**Polynomial Model**

# Origin of Spatial Correlation Dependence

- Within-die variation:

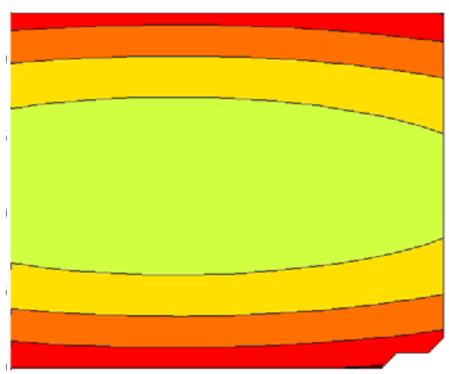



**Average Field**

**Scaled Mask Errors**

**Non-mask related across-field systematic variation**

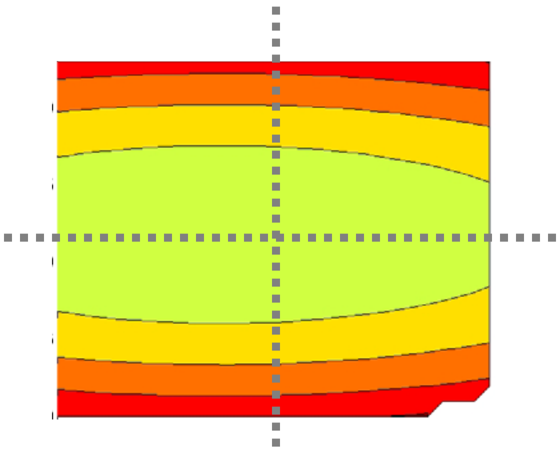
**Polynomial model of across-field systematic variation**

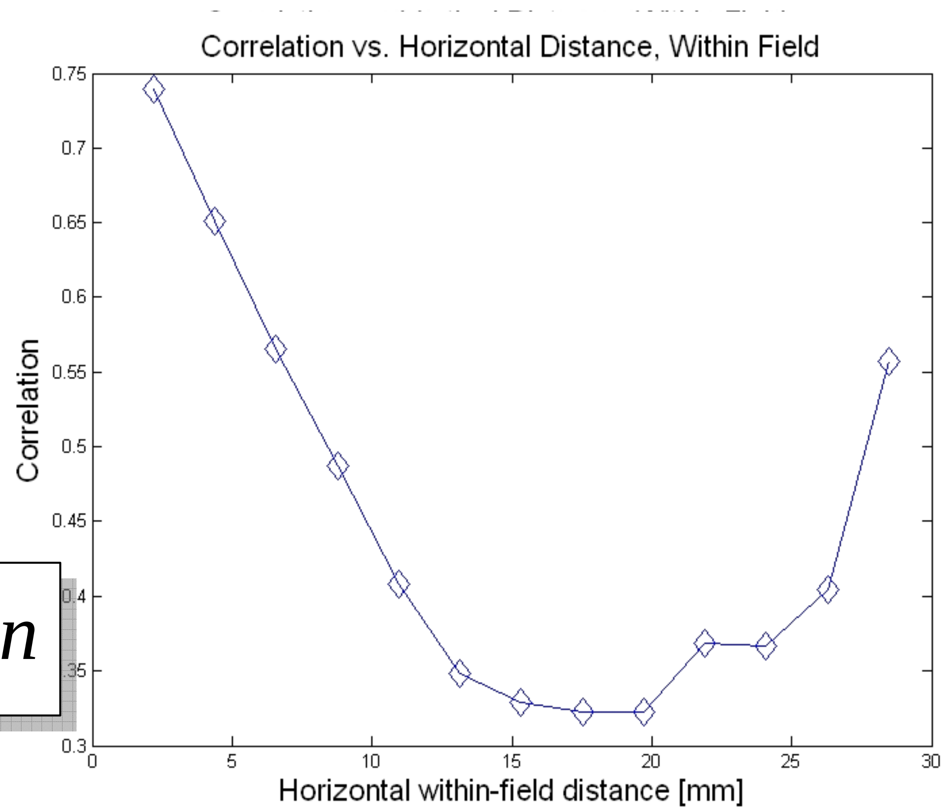


The "shape" of this model will be very similar to the "shape" of spatial correlation dependence.

# Origin of Spatial Correlation Dependence

- By slicing the within-die variation, we can see where the origin of the spatial correlation plots

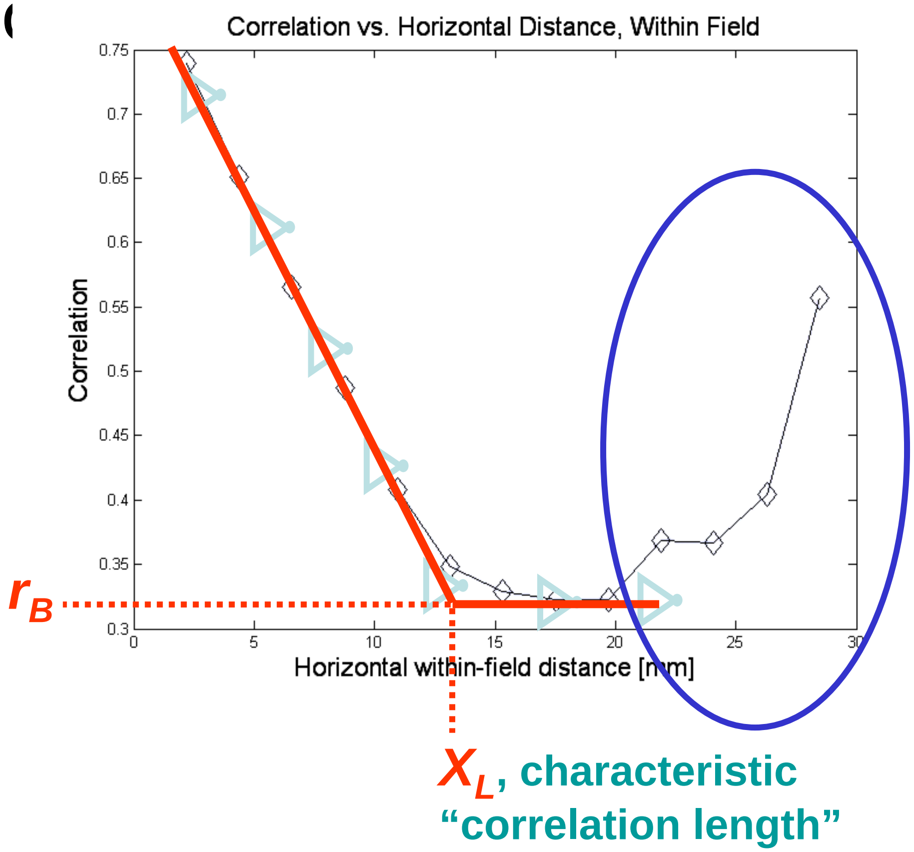





$$\rho_{jk} = \left(\sum z_{ij} * z_{ik}\right)/ n$$

# Spatial Correlation Model

- Fit rudimentary linear model to spatial correlati… …irical data:



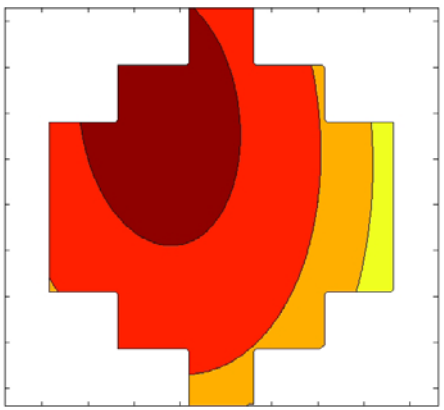

Characteristic "correlation baseline"

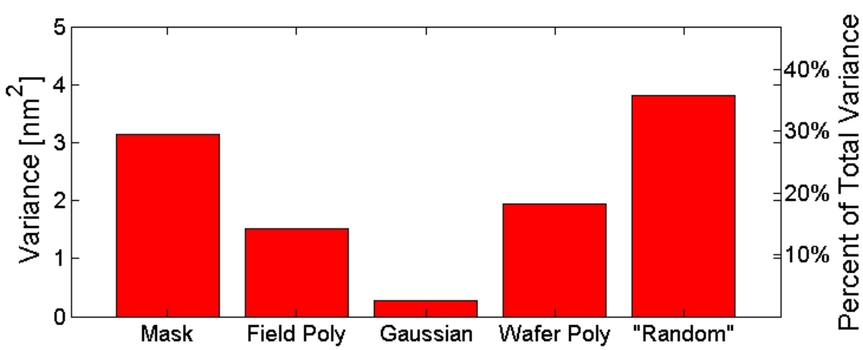
Ignore this part - distances to large for typical IC sub-circuit

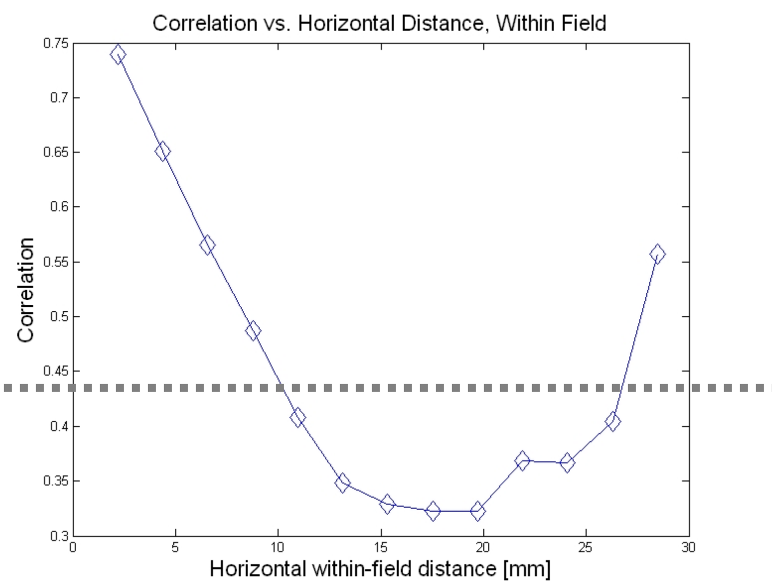
$X_L$, characteristic "correlation length"

# Origin of Spatial Correlation Dependence

- The across-wafer variation impacts $\rho_B$:






Relative "weights" of field & wafer variation determine overall shape of spatial correlation curve

# Calculation of Expected Effect

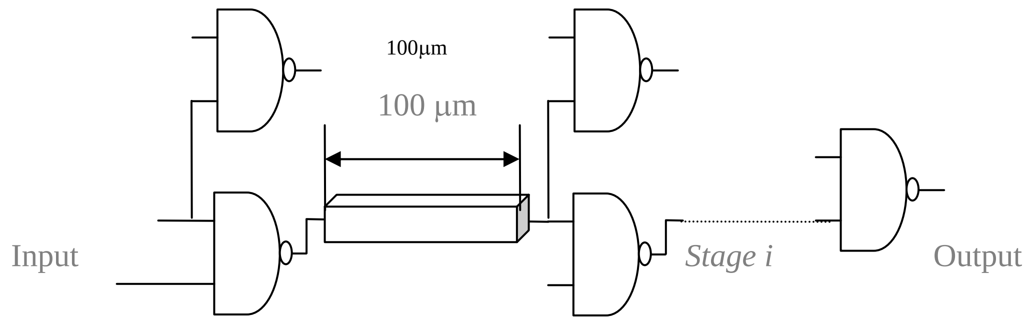
- Assuming *n* independent random variables with equal mean and variance, the variance of the sum of the *n* variables is:

$$\sigma^2{}_{tot} = n\sigma_{indv}{}^2 + 2\rho\left({}_nC_2\right)\sigma_{indv}{}^2 = \left[n + \rho(n)(n-1)\right]\sigma_{indv}{}^2$$

- For $\rho = 1$, $\sigma_{tot} = n\sigma_{indv}$
- For $\rho = 0$, $\sigma_{tot} = n^{1/2}\sigma_{indv}$
- Total potential improvement is factor of $n^{1/2}$ (i.e., for a 16-stage path, maximum total delay variation reduction is ~4x…)

# Monte Carlo Simulations

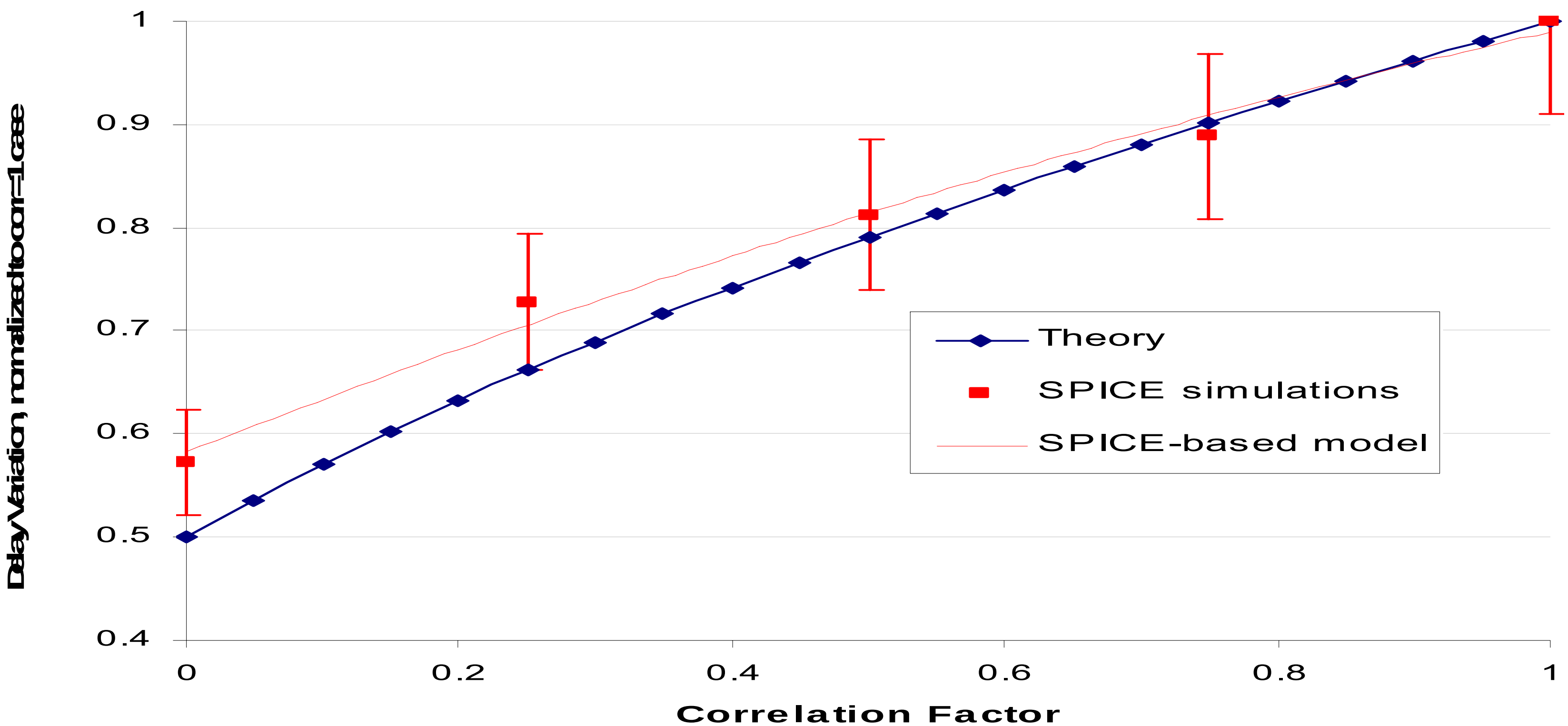
- Use canonical circuit of FO2 NAND-chain w/ stages separated by 100μm local interconnect, ST 90nm model:



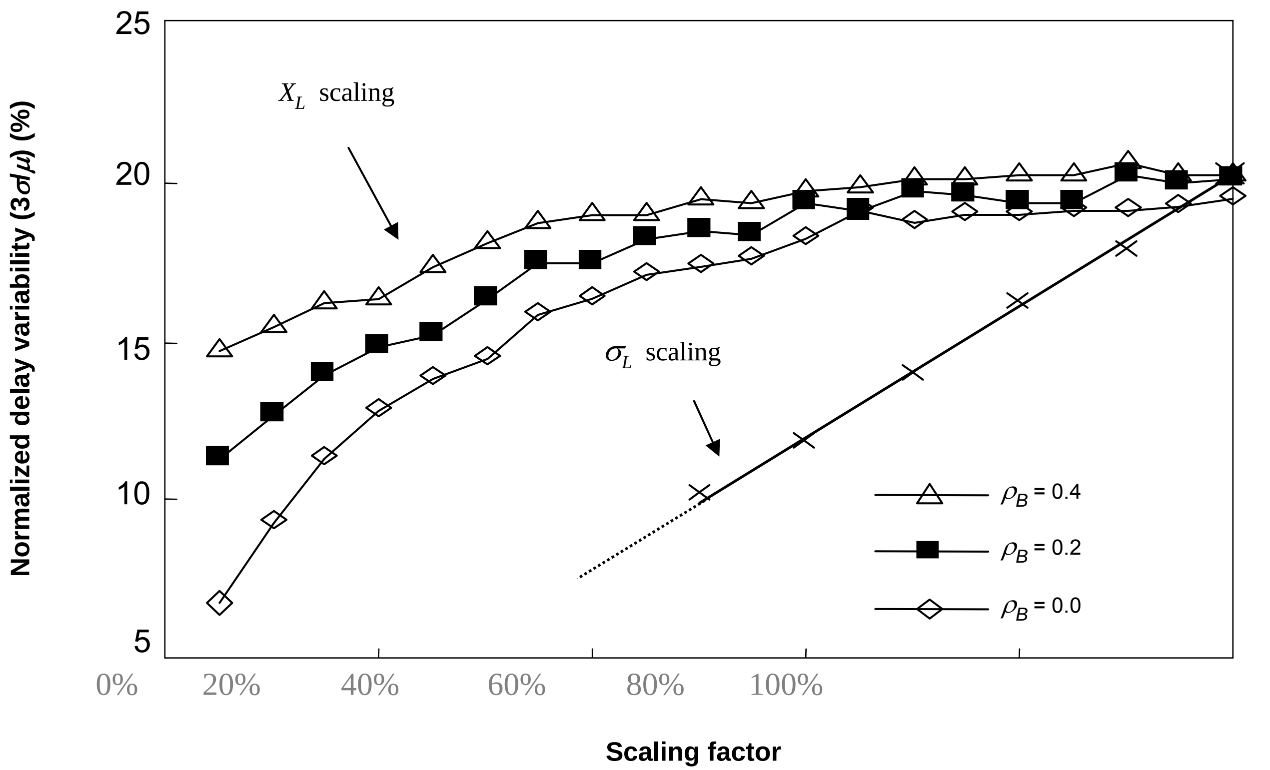

- Perform Monte Carlo simulations for various combinations of $X_L$, $\rho_B$, and $\sigma/\mu$ (gate length variation)
- Measure resulting circuit delays, extract normalized delay variation ($3\sigma/\mu$)

# Statistical Theory vs. Circuit Simulation

- Prediction of potential impact of spatial correlation using SPICE simulations on simple

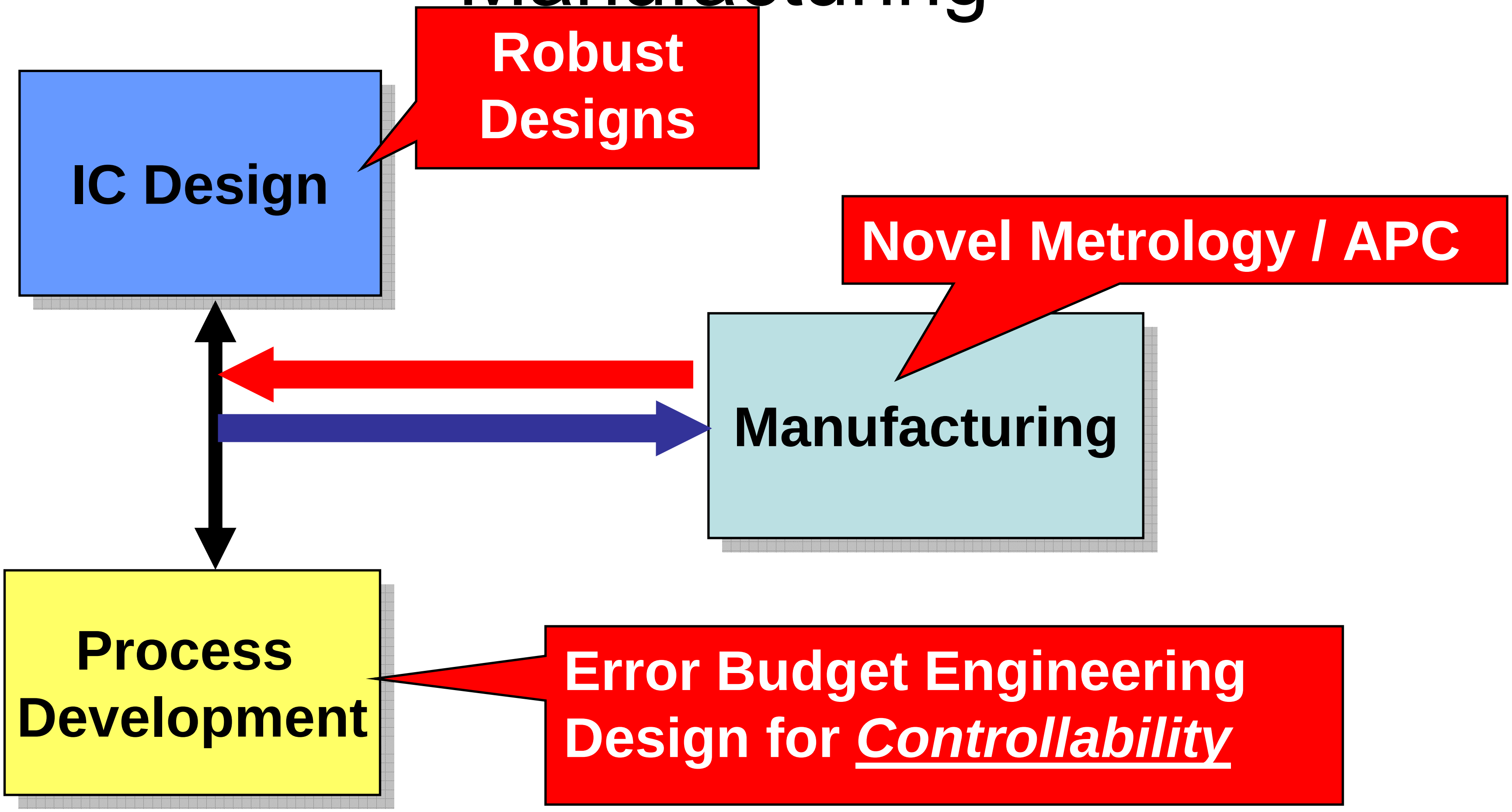


# Delay Variability vs. $X_L$, $\rho_B$, $\sigma/\mu$




- Scaling gate length variation directly has most impact
- Reducing spatial correlation also reduces variability

# Coping with Variability in Semiconductor Manufacturing



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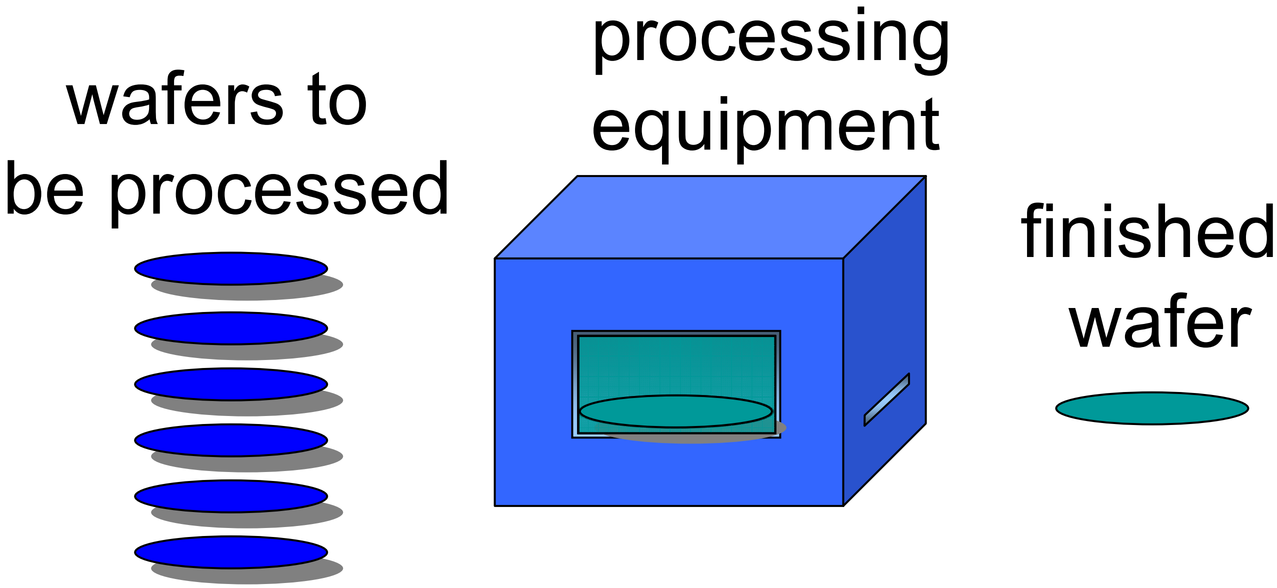
- Modeling Variability
  - Interaction of Design and Manufacturing
  - Design for Controllability

► Future Perspectives

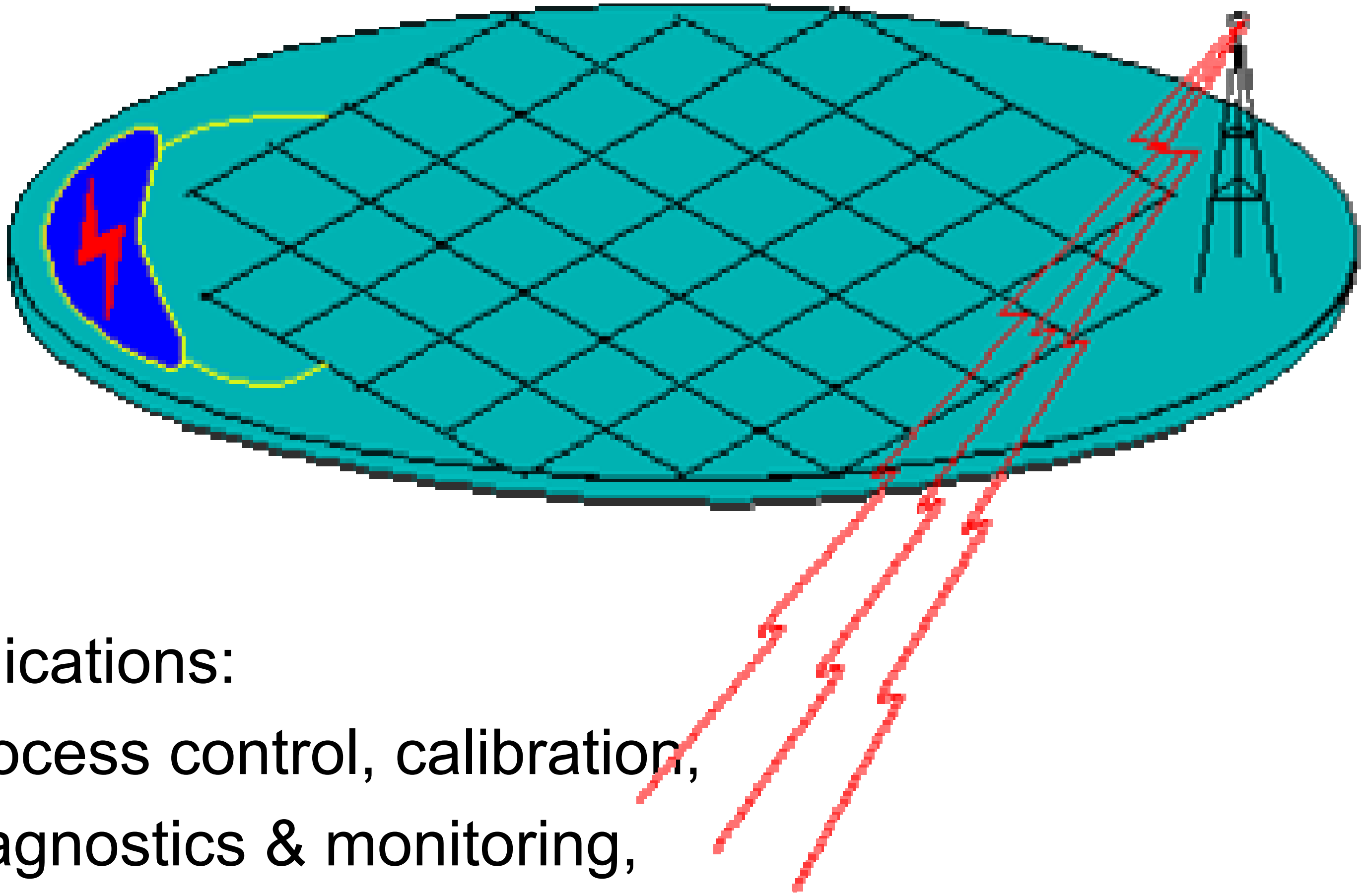
# Processing Sequence




What was the state of the wafer during processing?

# Smart Sensor Wafers

*In situ* sensor array, with integrated power and telemetry



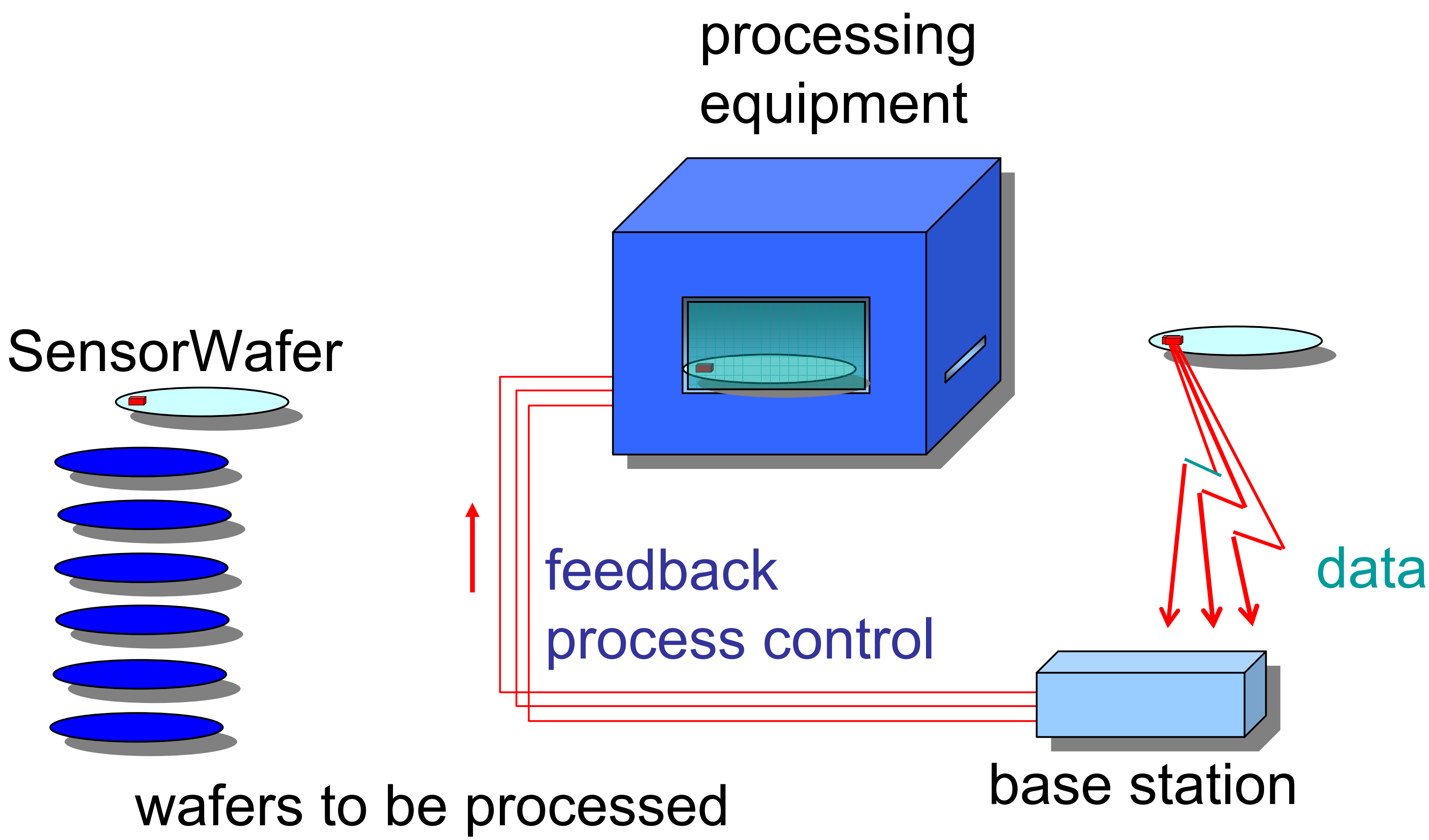
Applications:

process control, calibration,

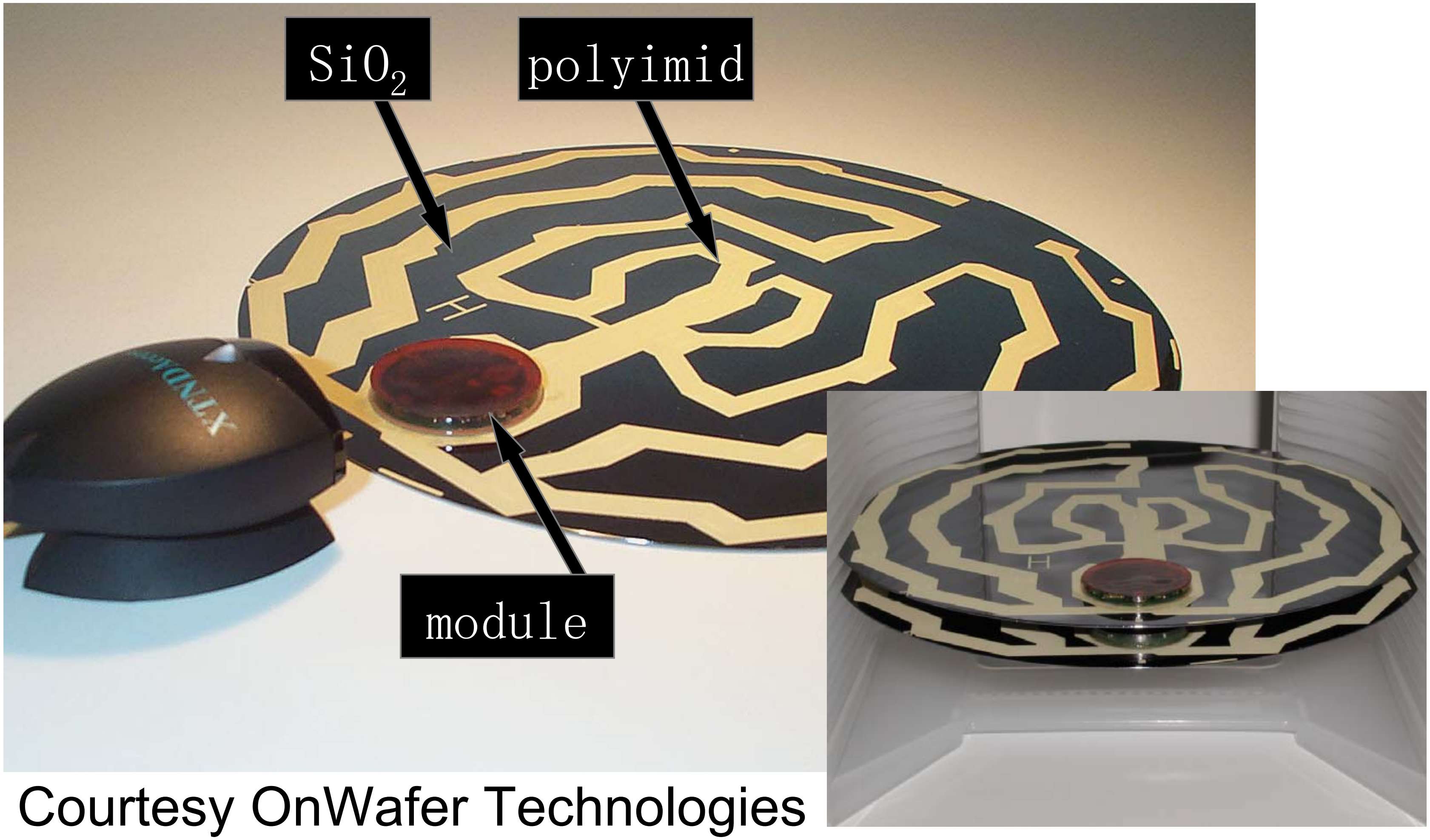
diagnostics & monitoring,

process design

# The Approach

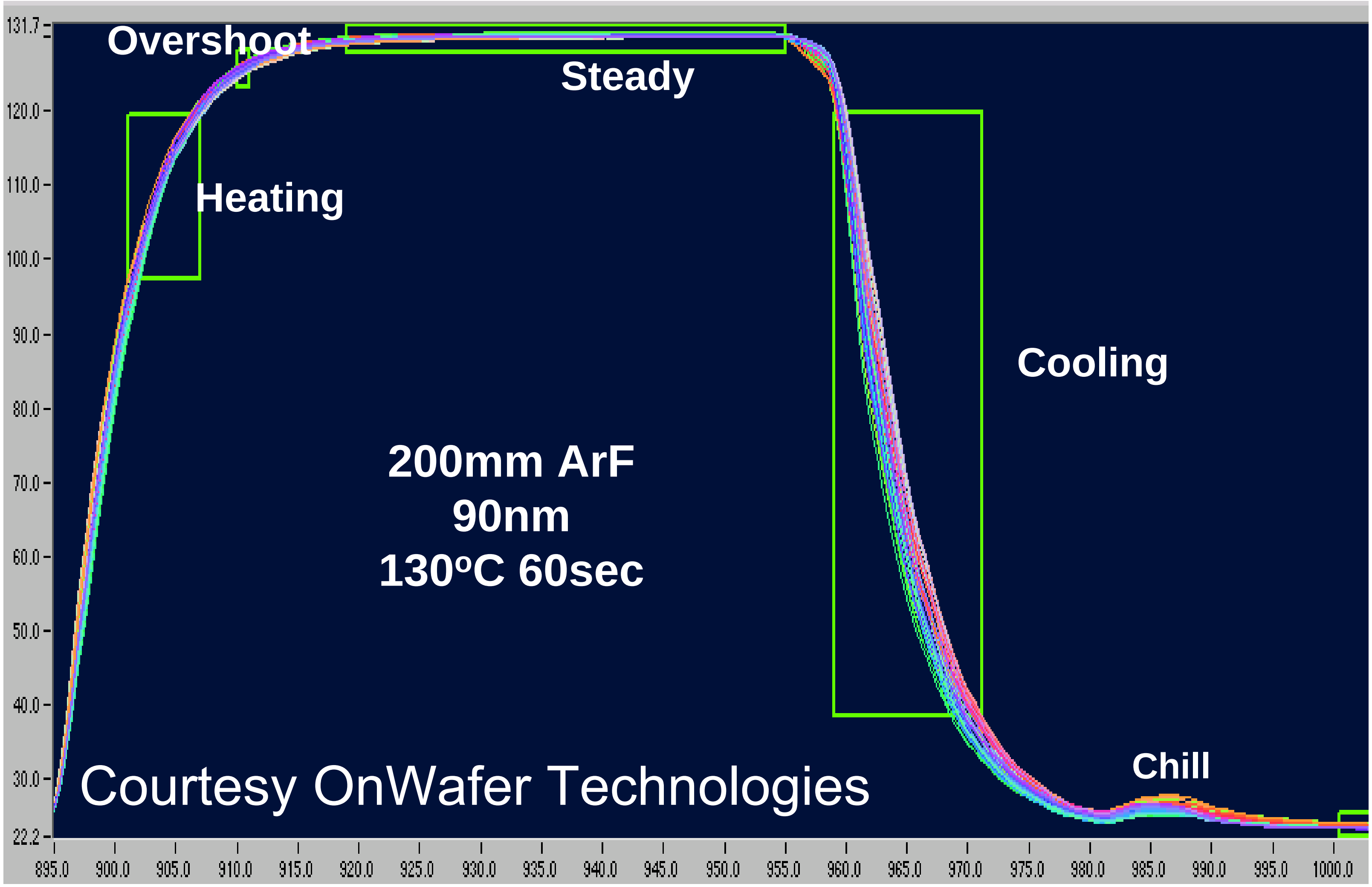


# Today: The Sensor Wafer

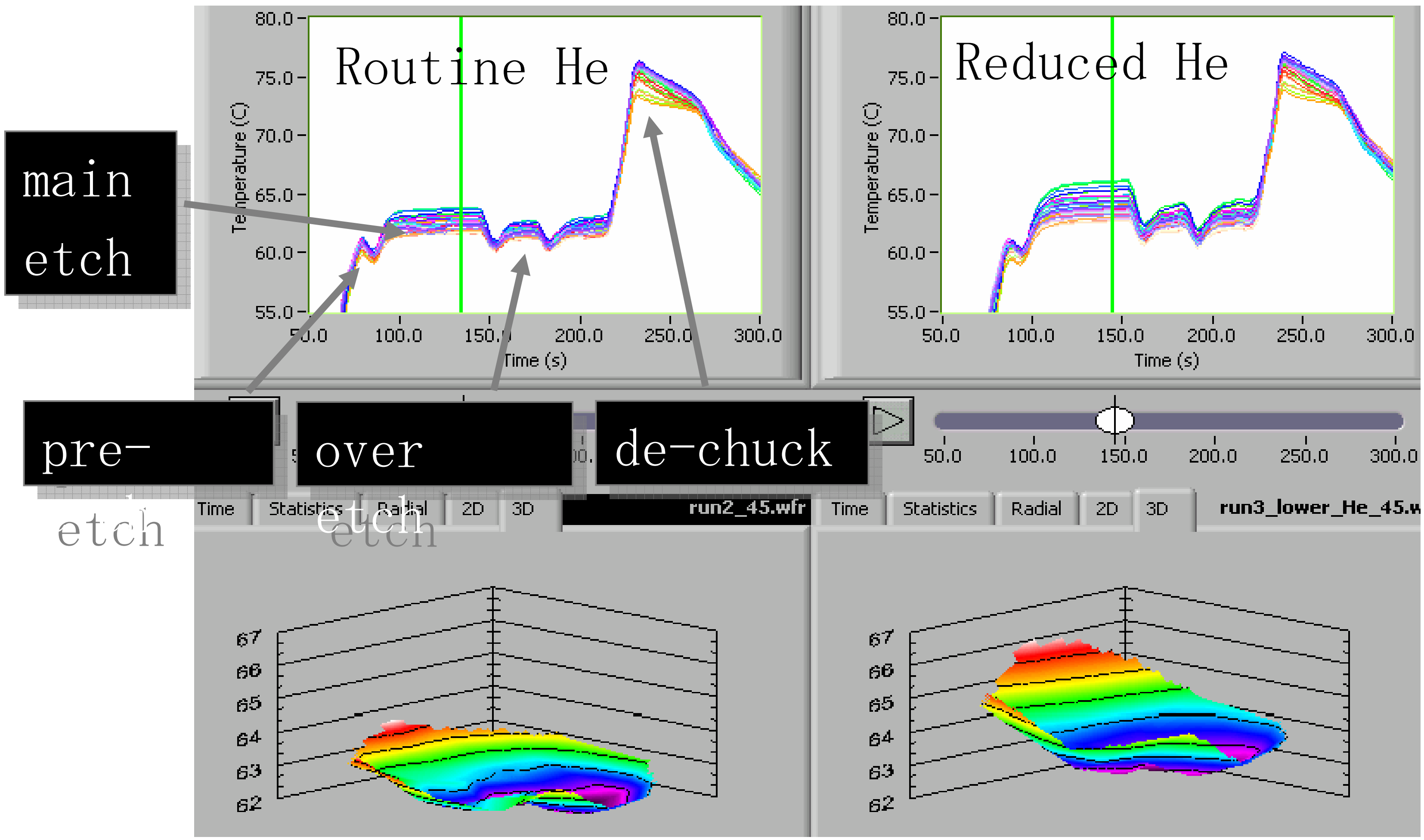



Courtesy OnWafer Technologies

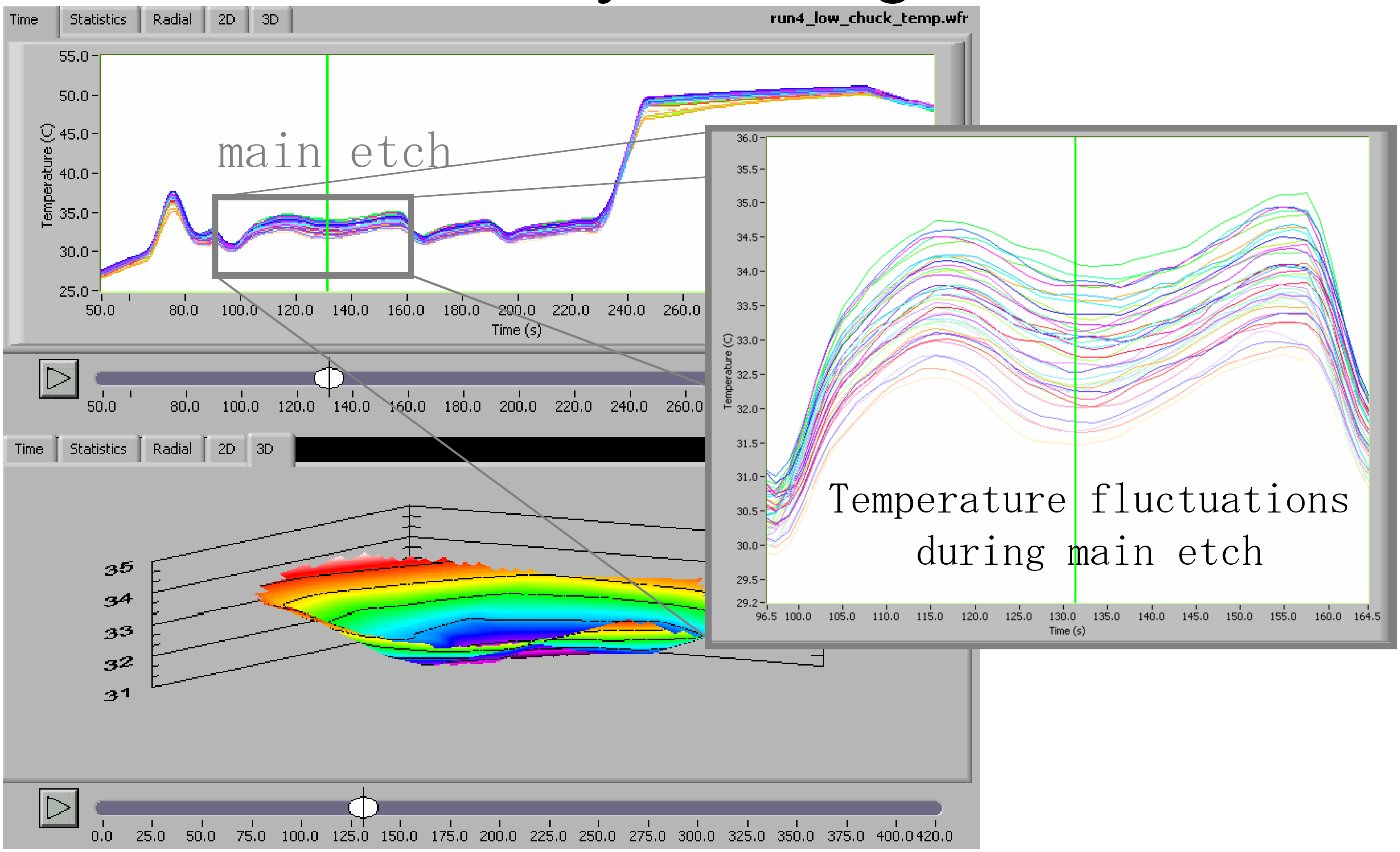
# Much more than you ever wanted to know about Post Exposure Bake



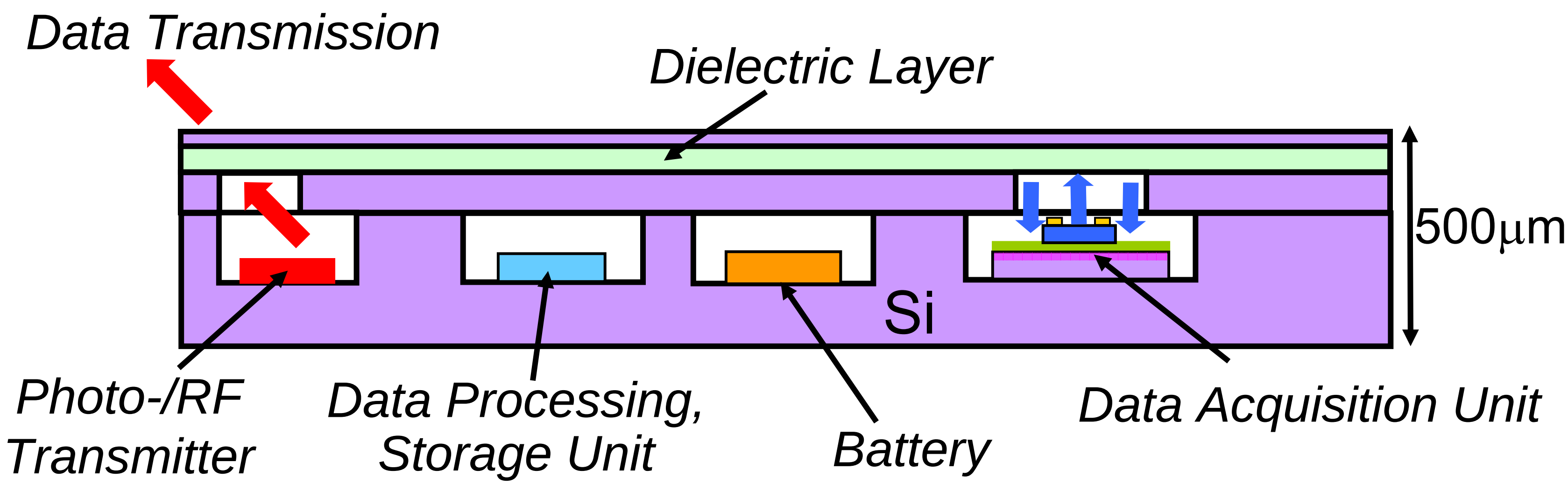
# On-Wafer Plasma Monitoring
# 200mm Poly Etching



# Cool chuck - 200mm
# Poly Etching

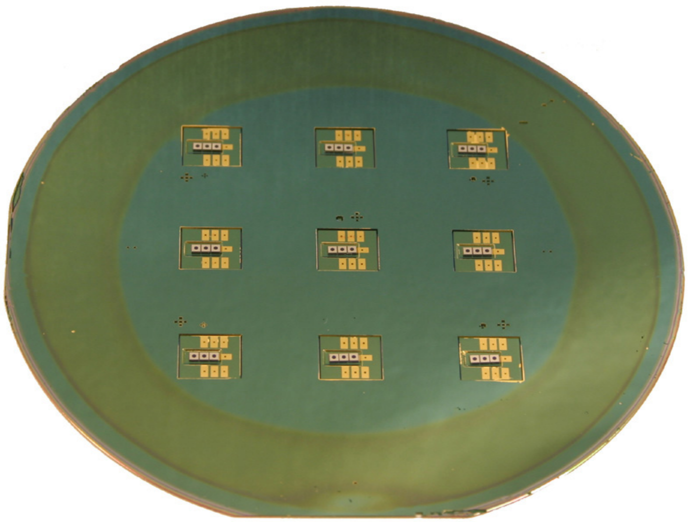


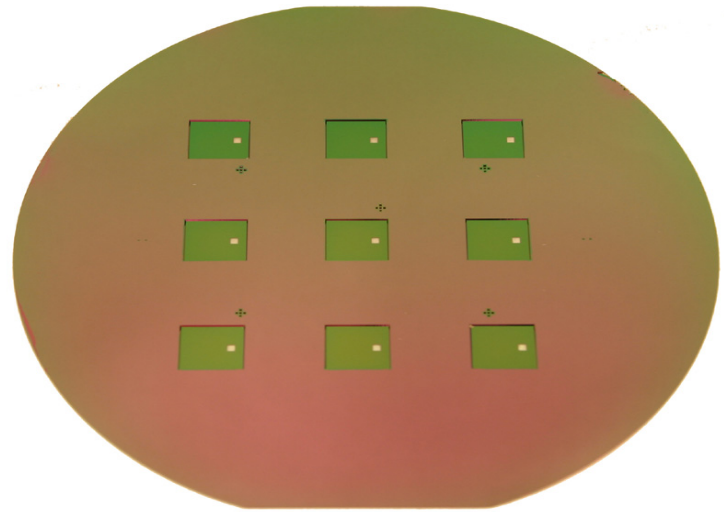
# Next Step: Zero-Footprint Metrology Wafer

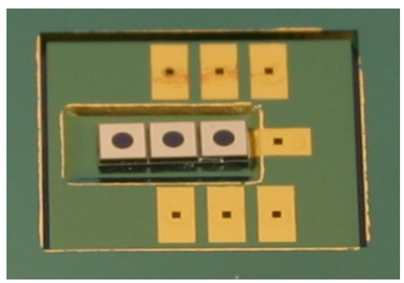


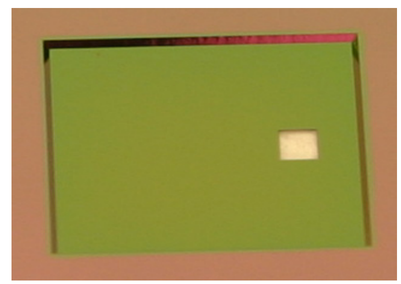

Prototyping a zero-footprint metrology wafer with optical detection unit and encapsulated power source.

# 3 x 3 Pixels Optical Metrology Prototype





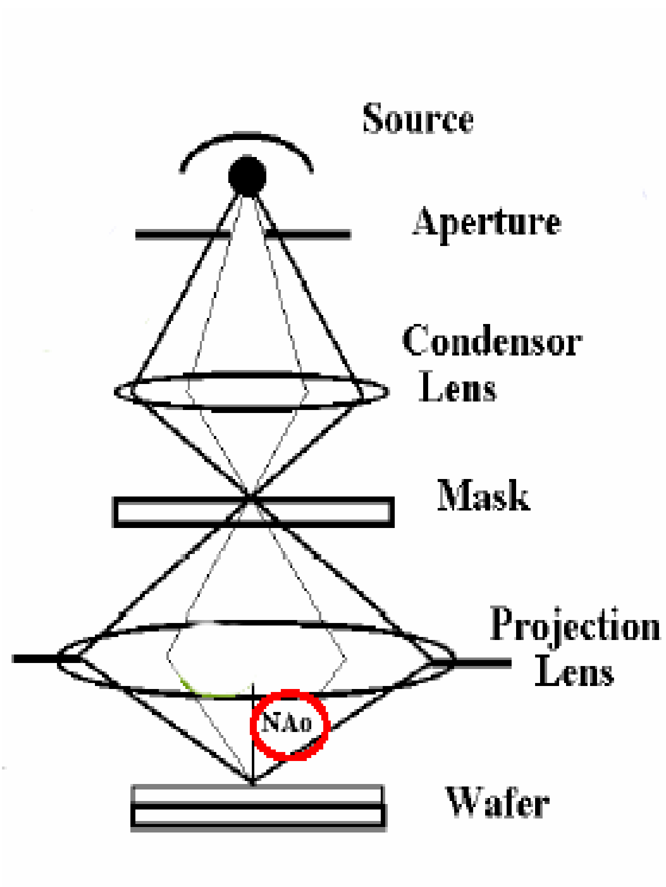


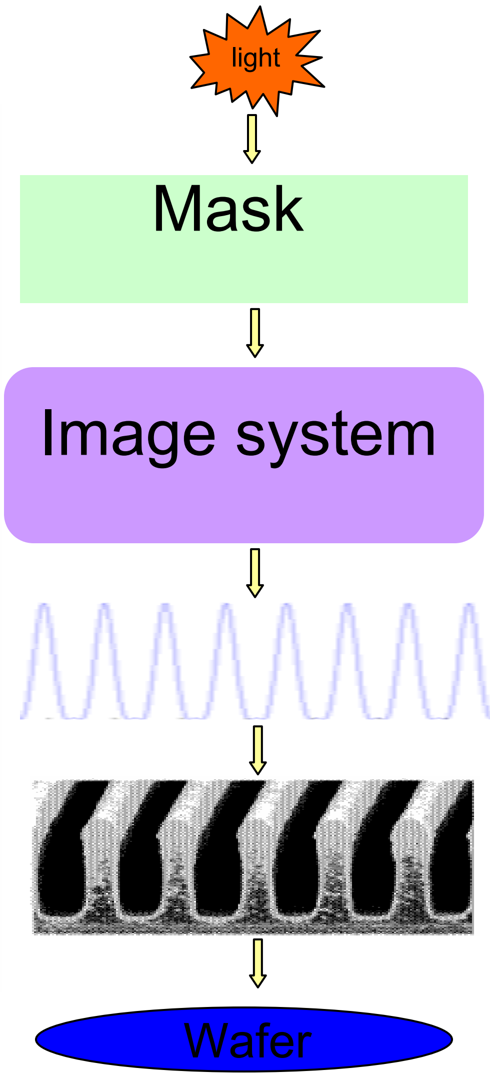


Bottom Wafer with LED Photodetector integrated

Top Wafer

# Wireless Aerial Image Metrology




Mask image

**NA**
**Partial coherence**
**Illumination aberrations**
**Defocus**
**magnification**

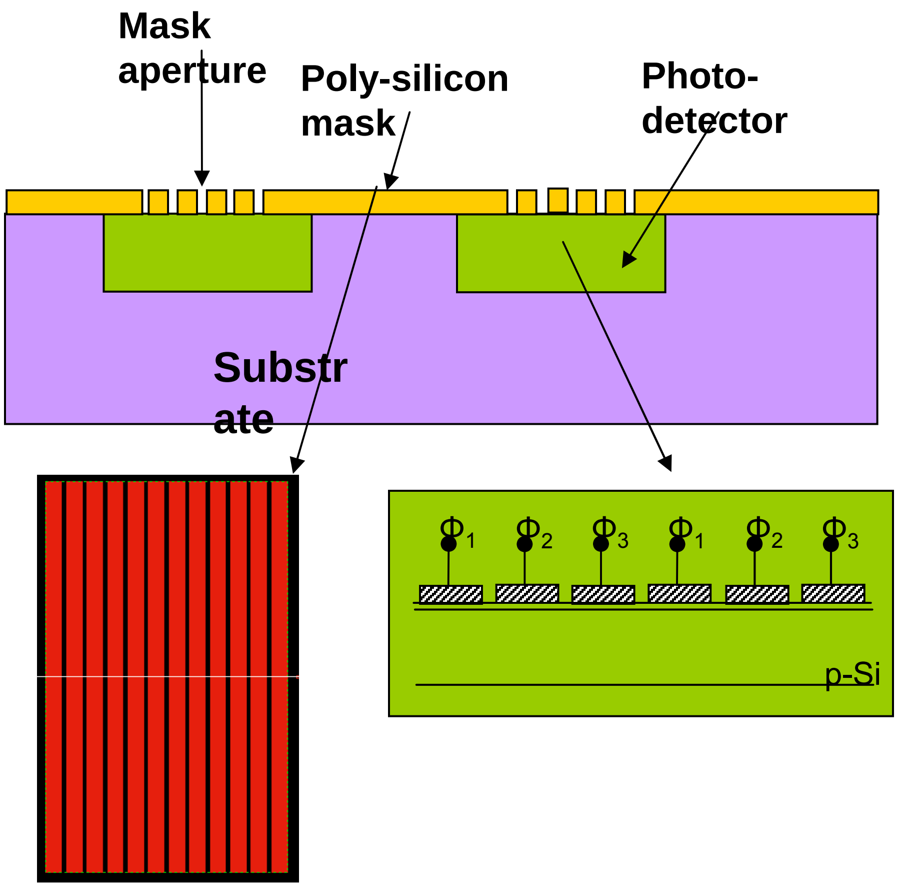
Aerial image

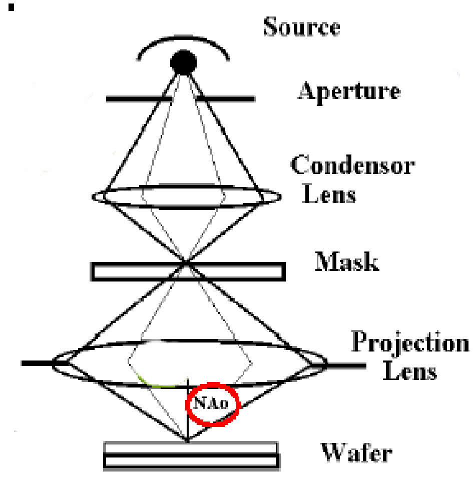
Latent image

Resist image

# An Integrated Aerial Image Sensor

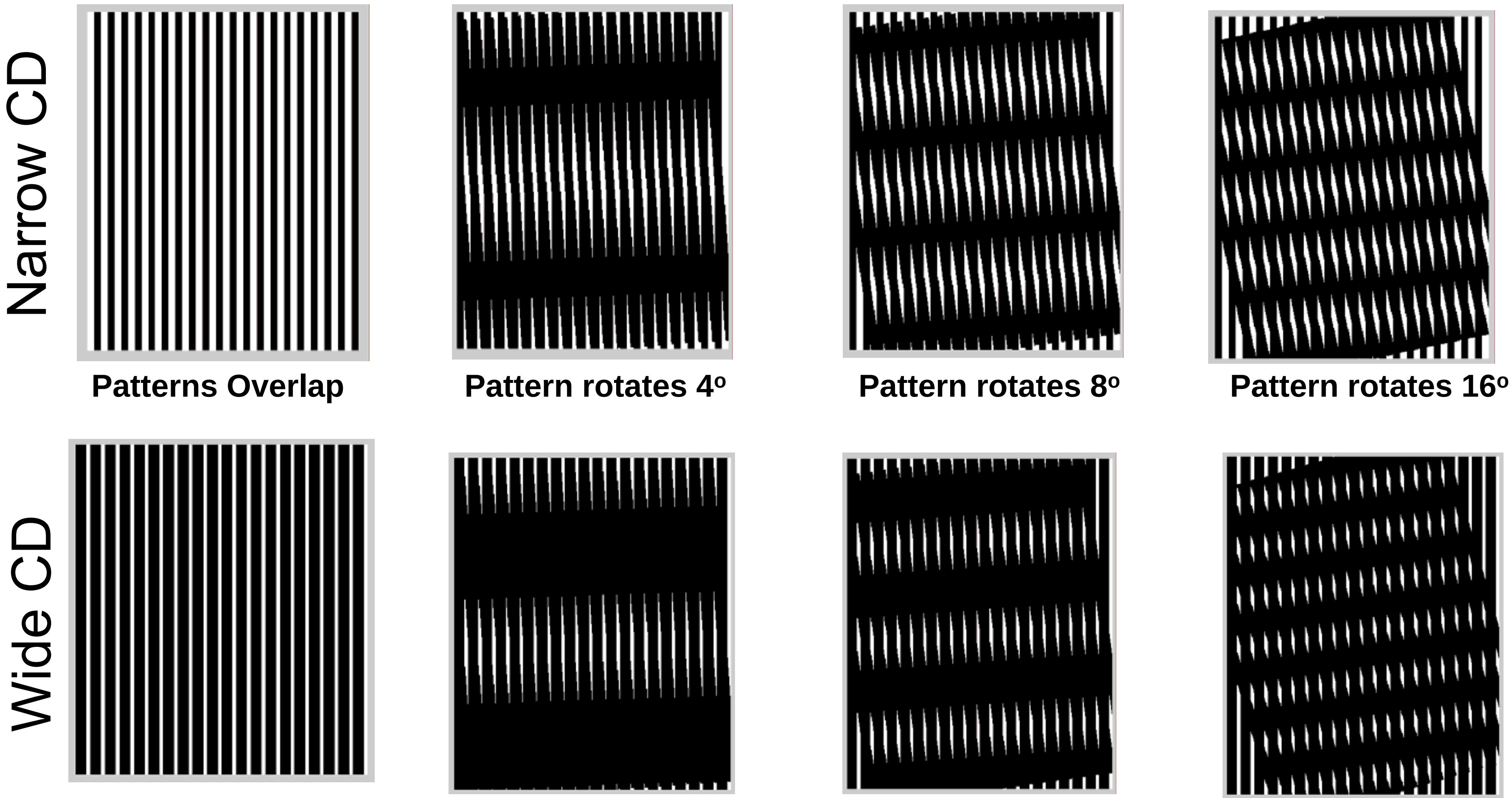
Dark contact mask forms a “moving” aperture to capture incident electromagnetic field.



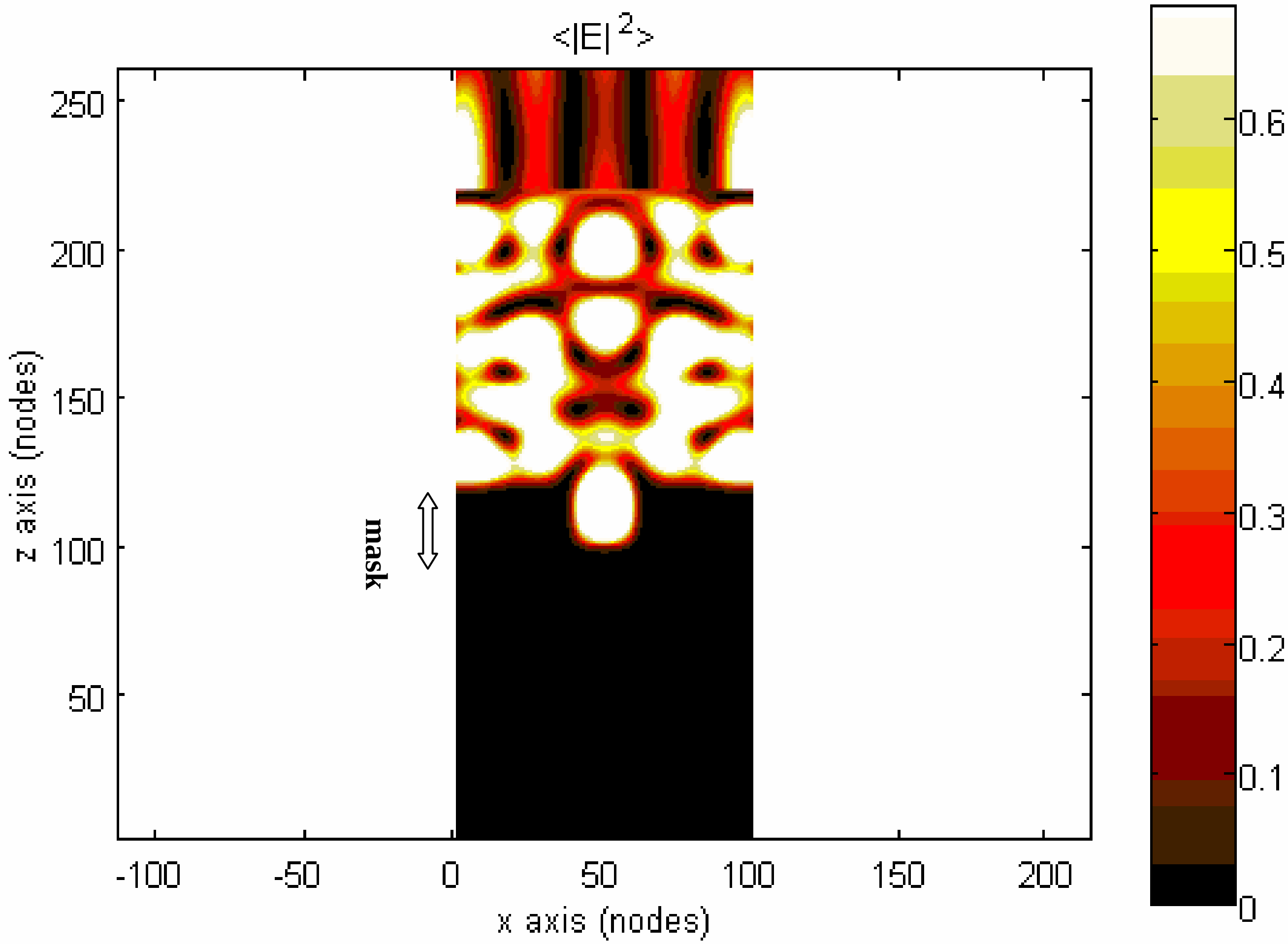




How can a μm detector retrieve nanometer-scale resolution of the aerial image?

# Moiré Patterns for Spatial Frequency Shift



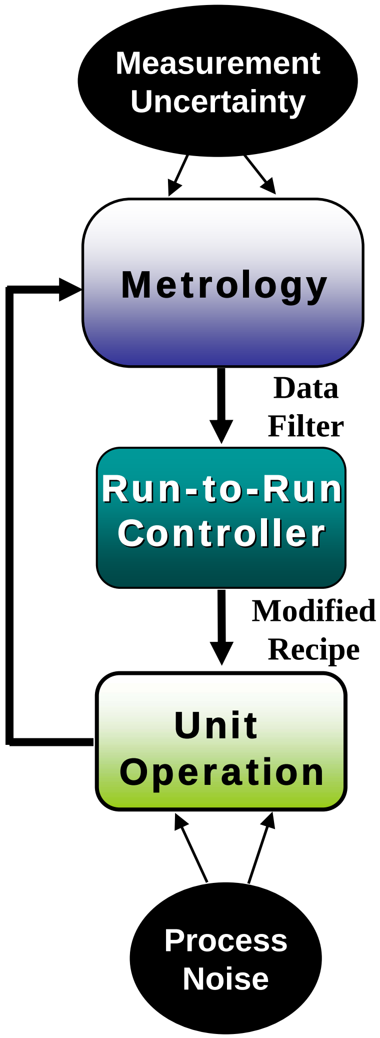
# Near-Field Optical Simulation




Intensity at the center of the simulation domain

# Metrology for APC
# *Why does APC care about metrology?*

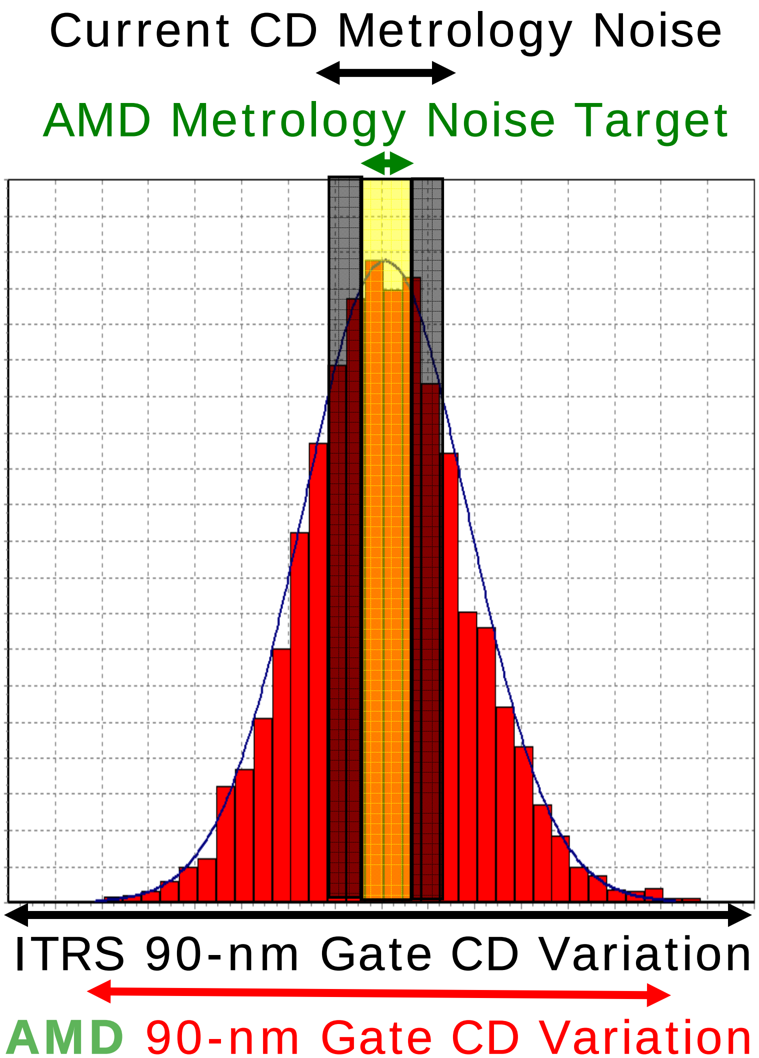
- Garbage-in, Garbage-out (GIGO)
  - Noisy metrology limits controller effectiveness
    - Controllers must filter, dampen and average the signal to account for noise
    - These actions may compromise control objectives or constrain the factory
  - Metrology errors become process errors
    - RtR controllers can not distinguish between metrology and process errors
    - The controller will adjust for a metrology trend or shift as if it were a process deviation
    - The result is a mis-targeted process
- No metrology means no APC
  - New control needs are emerging with no robust measurement solution
  - Metrology is the gating item to controller development



# Advanced Measurement Technology (AMT)

- The AMD APC roadmap can not be achieved without directly addressing metrology challenges
  - **Reducing Uncertainty**
    - **Improve existing metrology metrics to meet APC needs**
    - Metrology noise must be reduced (precision)
    - Metrology data must reflect real process variation (accuracy)
    - Metrology trends and shifts must be eliminated (stability)
  - **Creating new capabilities**
    - **Develop product metrics to enable new APC applications**
    - Pattern height and shape
    - Line roughness
    - Design-based Metrology
- The AMT team is dedicated to working with APC to destroy metrology roadblocks

# Gate APC and Metrology Precision

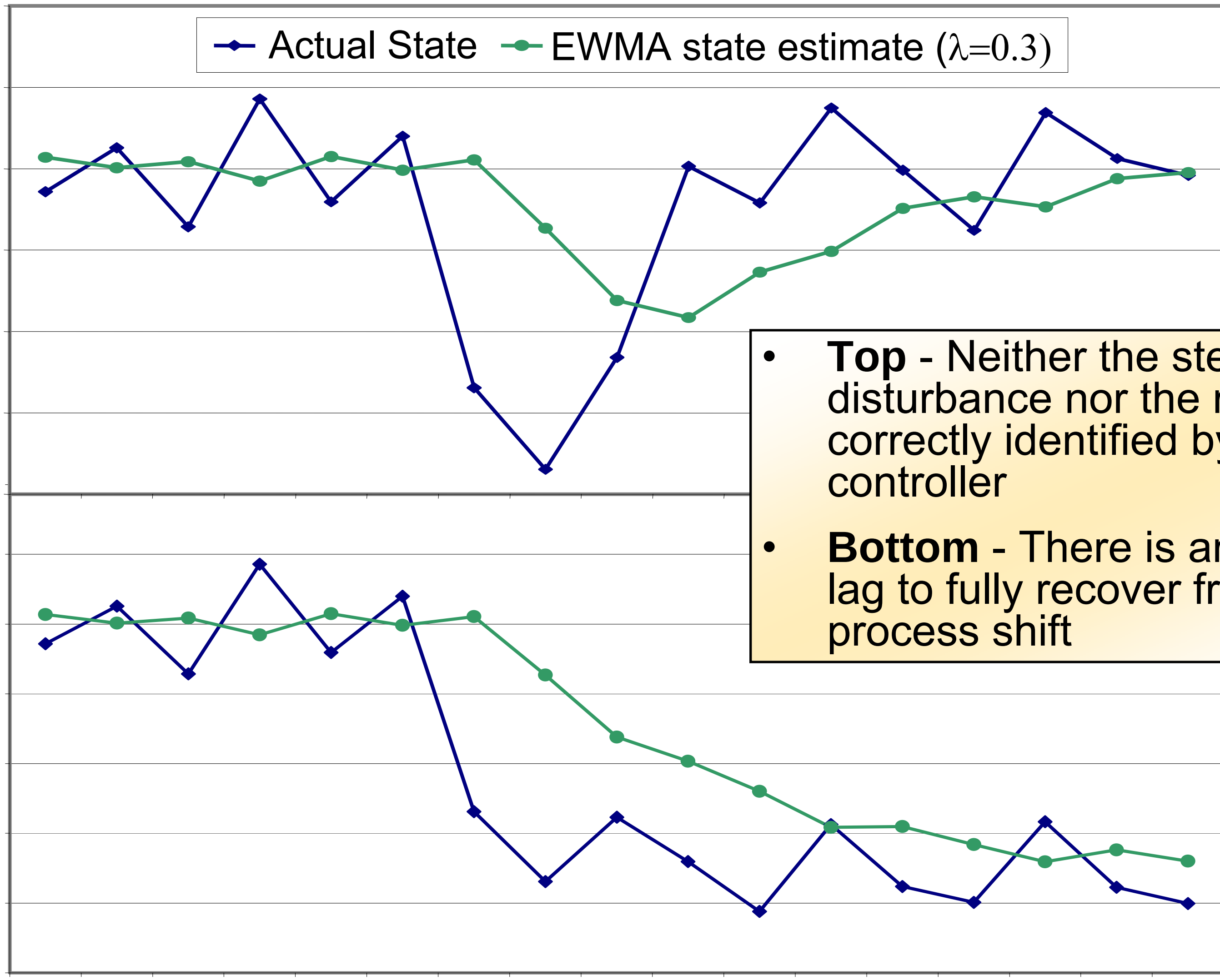



- CD-SEM metrology tools are meeting the ITRS spec for precision at the 90-nm node
- But gate etch RtR control has reduced the overall process range well below the ITRS benchmark
- Metrology precision is not adequate for these tighter process windows
- Metrology precision must improve by more than 100%!

# Managing the Precision Problem *with Algorithms*

- Mathematical methods to mitigate input noise:
  - Exponentially Weighted Moving Average (EWMA) state estimation
    - Averages the process state over time to ensure that the controller responds to a “real” signal
    - May hide some signals or delay detection of others
  - Statistical filtering (e.g. box filters) of incoming metrology data
    - Eliminates statistically erroneous measurements
    - May incorrectly ignore real process faults
  - Increasing the metrology sample size
    - Additional measurements increase confidence in statistics
    - Also burdens the factory with metrology cycle time

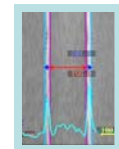
# Disturbances and EWMA Filtering

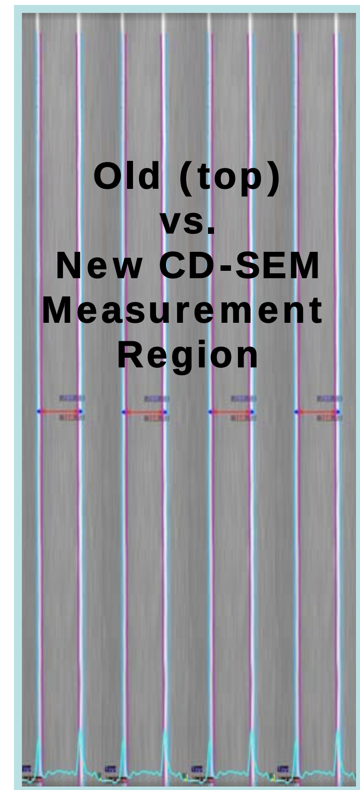



- **Top** - Neither the step disturbance nor the recovery is correctly identified by the controller
- **Bottom** - There is an eight run lag to fully recover from this process shift

# Managing the Precision Problem
## *with Advanced Measurement Technology*

- Identify key areas where control improvement is limited by measurement noise
  – CD metrology
  – Step height metrology
- Focus on improving the metrology rather than manipulating control algorithms
  – Implement rigorous metrology tool controls
    - With engineering focus and advanced equipment monitoring, CD-SEM precision can reach 2x of manufacturer's specifications
  – Drive supplier roadmaps for improved hardware and software
    - New SEM columns and measurement algorithms allow 100x more signal averaging than previous generation of tools
  – Investigate paradigm-shifting emerging technologies
    - Scatterometry has displaced the profilometer for STI step-height metrology and is challenging the CD-SEM on other fronts

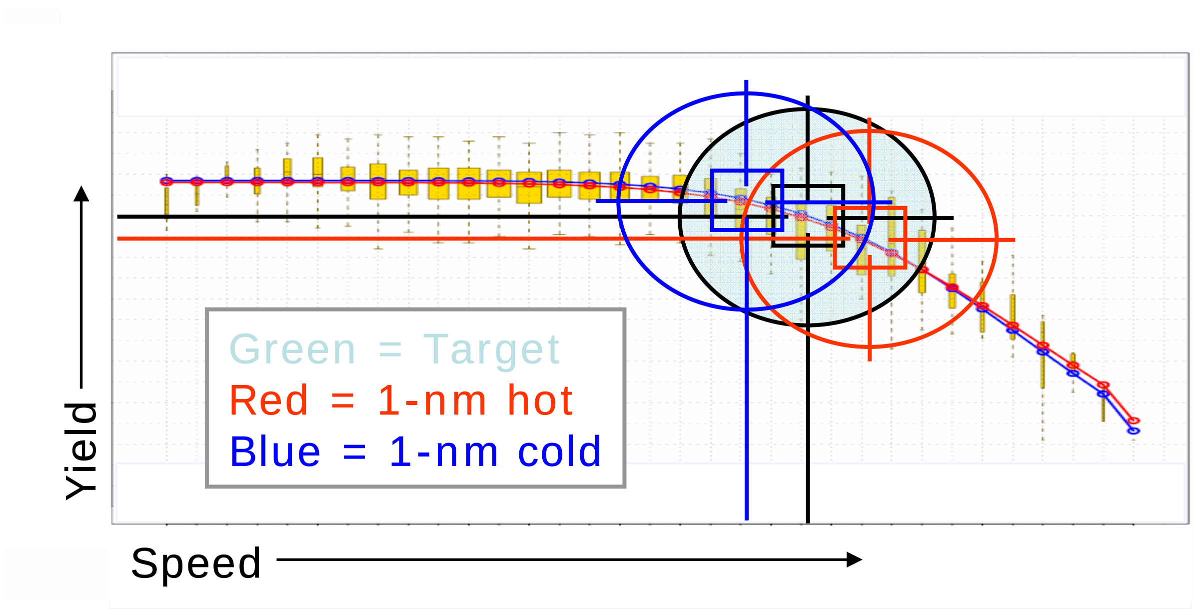


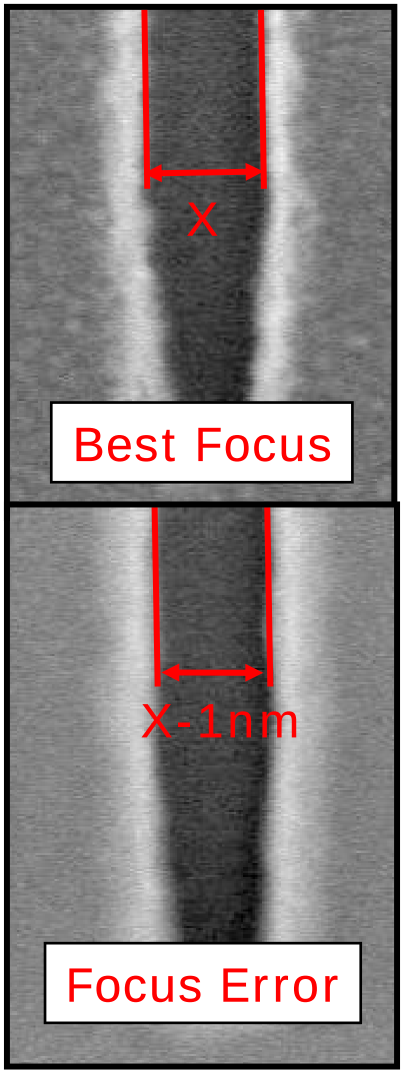


# Improving Measurement Stability

## *Gate CD Control*

- Slight variations in SEM imaging can cause metrology errors (like focus variation in these SEM images)
- A shift in CD distributions as little as 1-nm can lead to dramatic yield or speed degradation
- With APC control active and tolerances so severe, *metrology error must be eliminated*

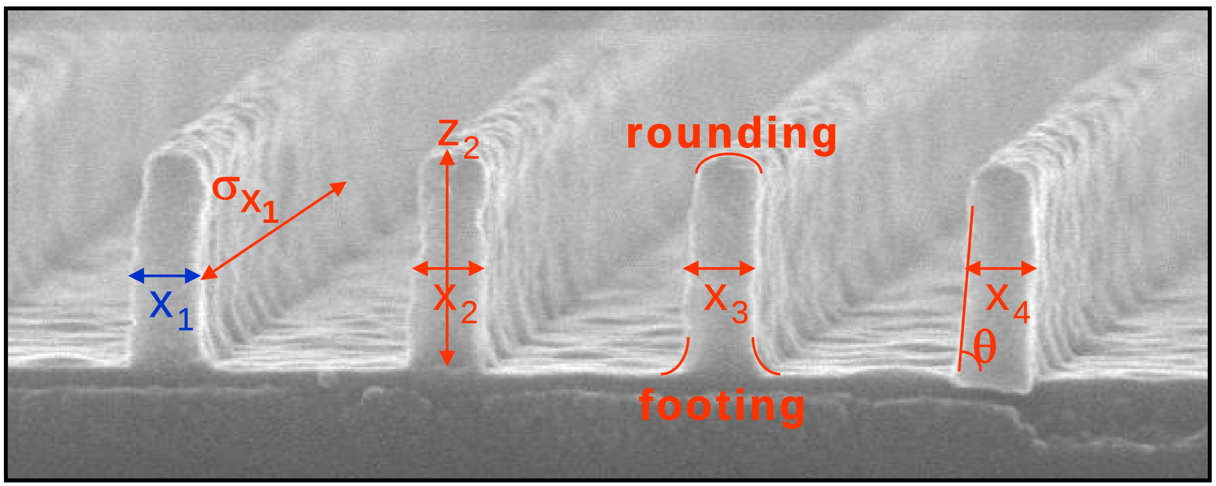


# Creating New Capabilities
# *Pattern Fidelity Metrology*

- For 90-nm and beyond, it is not enough to know the width of a single printed line
- Robust litho metrology must be able to answer the question:

  *"How accurately did I reproduce the mask pattern in all three dimensions?"*
- **Old Paradigm:** What is the CD of this array?
  - Metrology: point solution CD ($X_1$)
- **Beyond 90-nm:** What is the **pattern fidelity** of this array?
  - Metrology: 3-dimensional details ($X_{1\text{-}4}$, $X_{bar}$, $\sigma_x$, $\theta$, Z, footing, rounding)



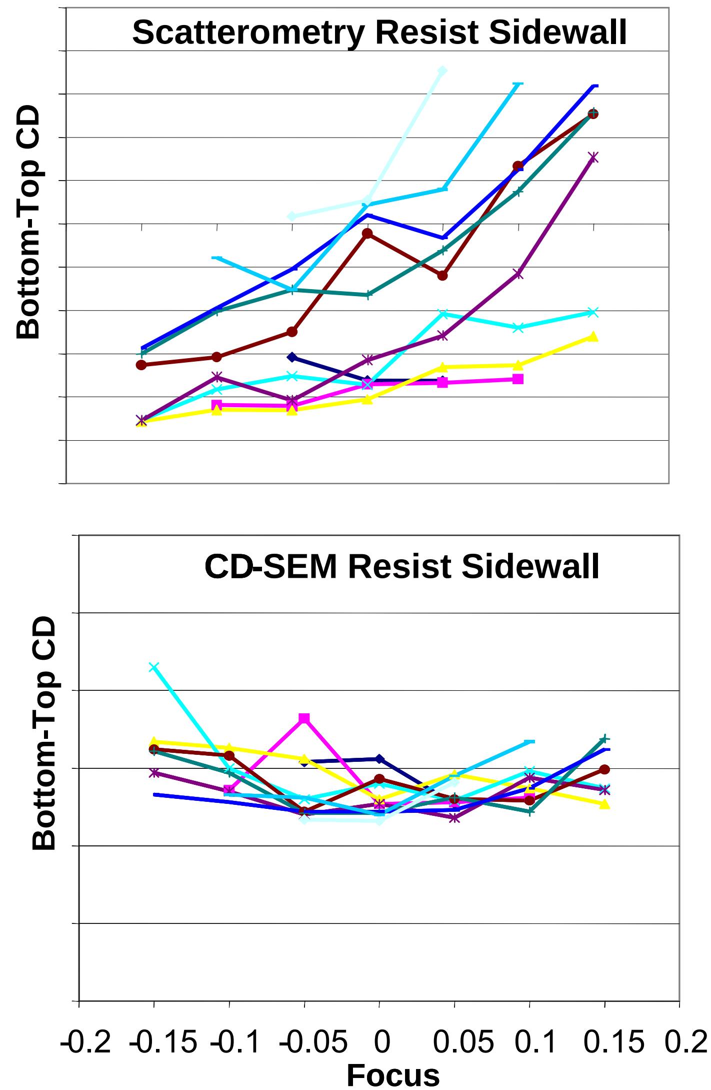

**Cross-section SEM image of 90-nm gate resist lines.**

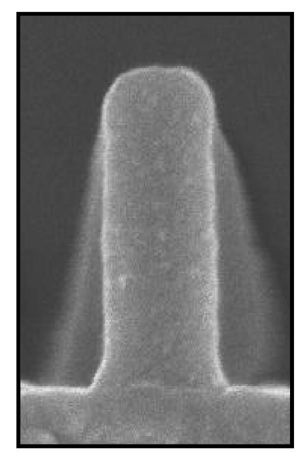
## Pattern Fidelity Tools

- Advanced SEM
  - $X_1$,$X_2$, $X_3$, $X_4$ or $X_{bar}$
  - $\sigma_{x1}$ (roughness)
- Scatterometry
  - $\theta$, Z, $X_{bar}$
  - Rounding/footing
- AFM
  - X, Z, $\theta$(?)
  - Reference metrology

# Creating New Capabilities
## *Sidewall Angle Metrology ($\theta$)*

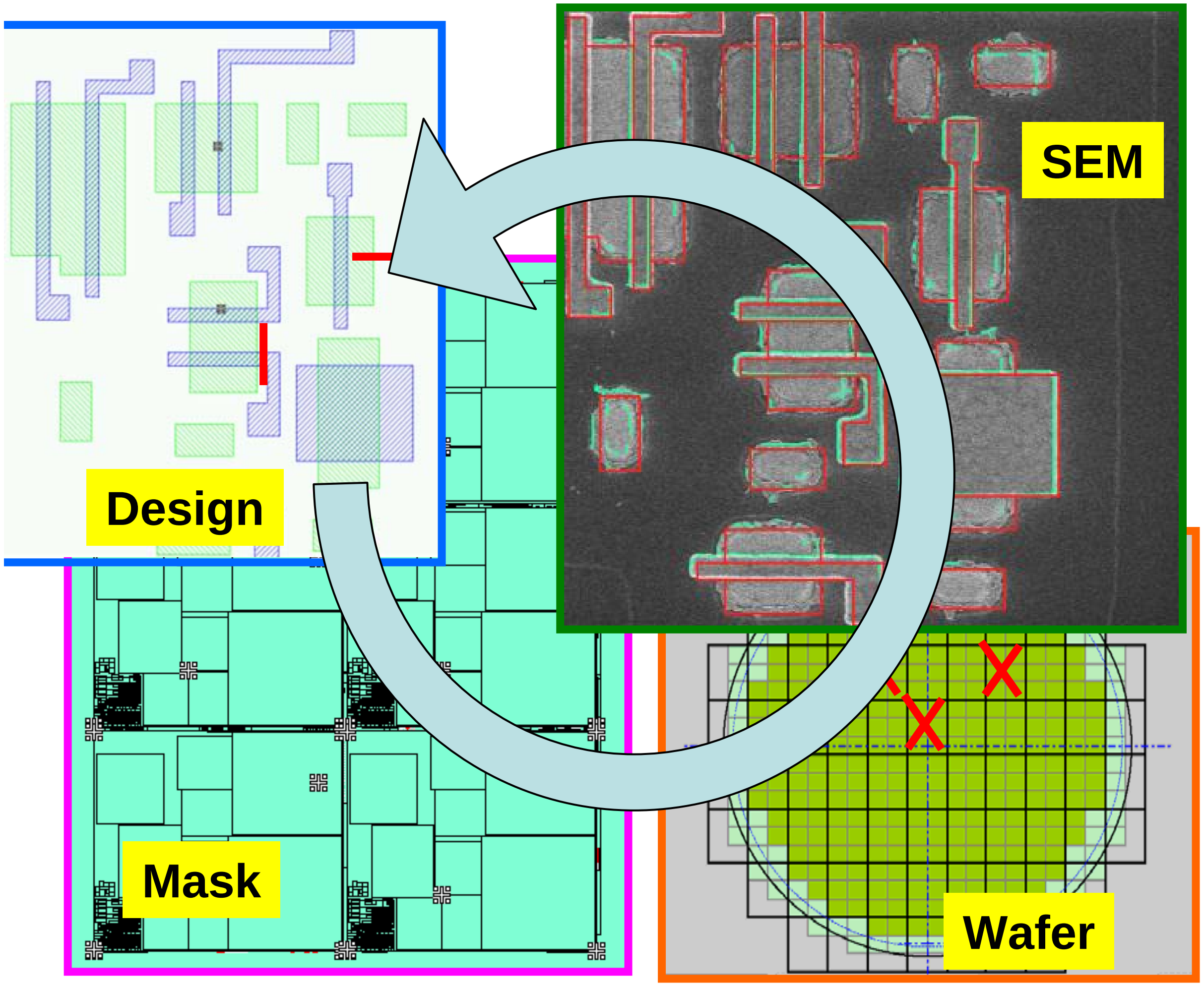
- Most scatterometry models return the sidewall angle of the feature
- The CD-SEM is incapable of measuring sidewall variation, especially for vertical profiles
- Sidewall data is a critical early indicator of focus error
- AMD APM is using scatterometry to develop integrated dose and focus RtR control



# Creating New Capabilities

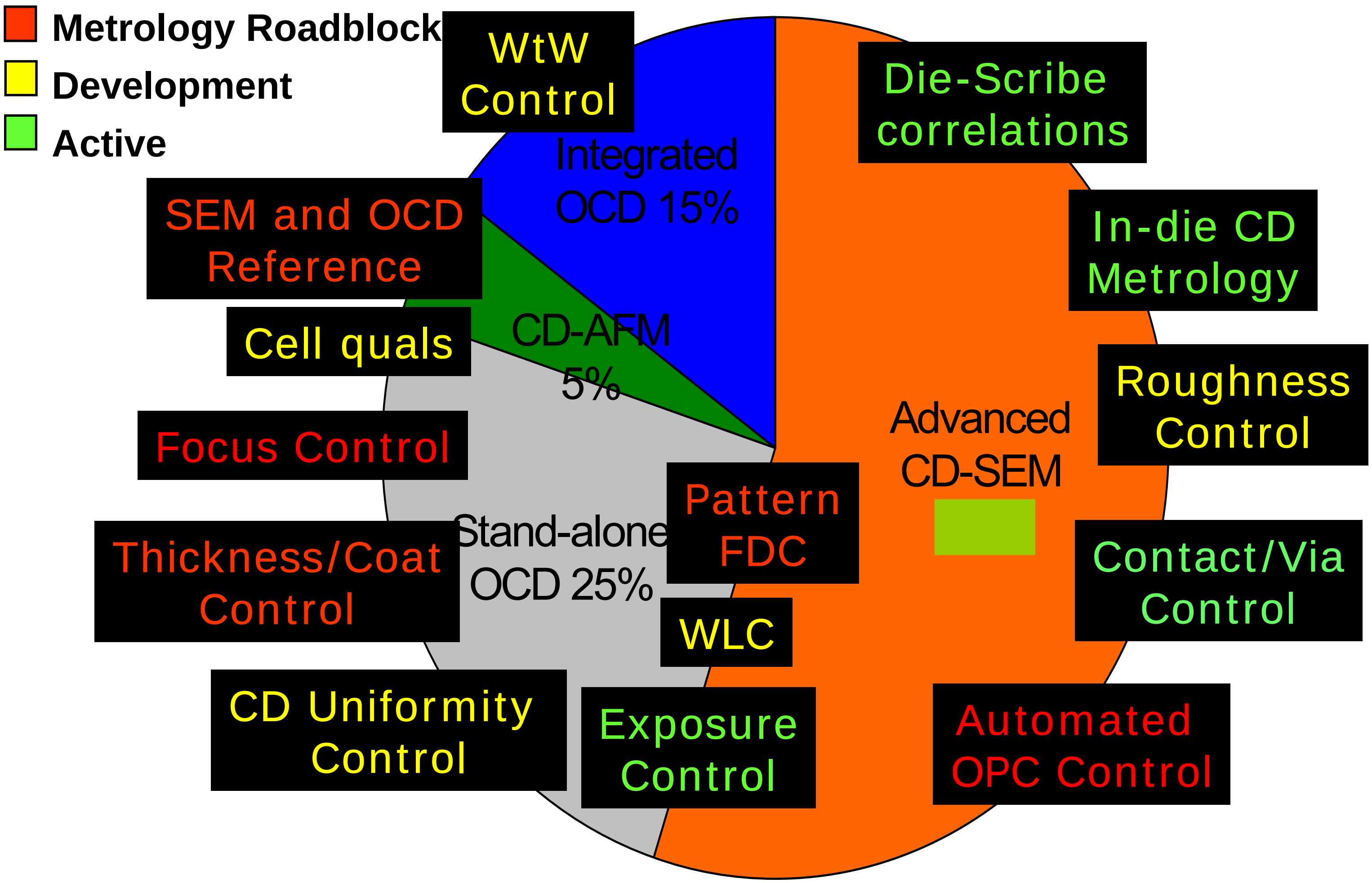
## *Design-based Metrology*




- Shrinking pitch and CD targets have forced complex lithography strategies (RET)
- One implication of RET is large proximity effects
- Optical Proximity Corrections (OPC) are designed into the mask to make the wafer image match design intent
- OPC model building and validation requires thousands of wafer measurements
- AMT has collaborated with the OPC community to create SEM recipes automatically from design data
- The SEM will soon be able to score the agreement between wafer and design and give numerical feedback
- The next frontier for APC???

# APC Lithography Applications

*We need AMT!*



# Conclusion

- APC technology  relies heavily on metrology development
  - Reducing the uncertainty of existing RtR input data streams
  - Developing new metrics to enable next-generation APC solutions
- It is naïve to believe that APC can address metrology deficiencies with advanced algorithms alone
- APC and the metrology community must work hand-in-hand to develop, test and implement new advanced measurement technology (AMT)
- The coordination of APC and AMT is a central element in AMD's Automated Precision Manufacturing (APM) strategy